EXHIBIT 8

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

U.S. Patent No. 10,510,842	Accused Products AMS-OSRAM TMF8828 configurable 8x8 multi-zone Time-of-Flight Sensor
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a semiconductor device. This chart includes exemplary information regarding a representative example of the AMS-OSRAM Accused Products, the AMS-OSRAM TMF8828 ("TMF8828"). The TMF8828 was analyzed in the below-referenced report from Tech Insights. The complete report is hereby incorporated by reference into each and every claim and claim element discussed. "AMS-OSRAM TMF8828, 17 µm × 39 µm Pixel Pitch d-ToF Sensor from Honor Magic3 Pro Rear-Facing Camera Device Essentials Plus Summary," *available at* https://library.techinsights.com/search/device-details?tab=reports&id=DEP-2110-801&genealogyCode=HNR-ELZ-AN10_ToF&activeTab=Reports ("TMF8828 Report"). Selected pages are reproduced herein to aid in understanding. Tech Insights techinsights.com ams OSRAM TMF8828, 17 µm × 39 µm Pixel Pitch d-ToF Sensor from Honor Magic3 Pro Rear-Facing Camera Device Essentials Plus Summary TMF8828 Report at Cover. The AMS-OSRAM TMF8828 is representative of the AMS-OSRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other AMS-OSRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, the other AMS-OSRAM Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). Similarly, the other AMS-OSRAM Accused Products would have been designed in a similar manner as the AMS-OSRAM TMF8828 for purposes of this claim chart to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828 transistors depicted here, and function in a

similar way with respect to the features claimed in the asserted claims, and the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828, and function in a similar way with respect to the features claimed in the asserted claims.

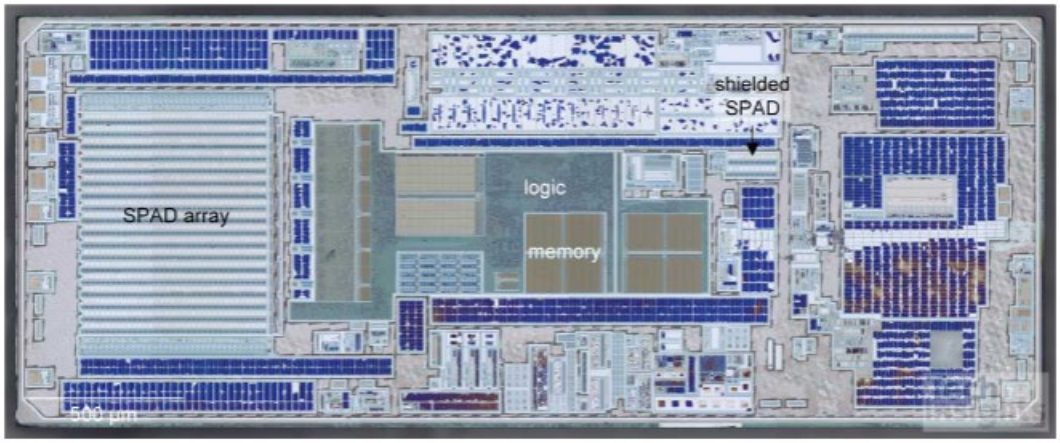
This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The AMS-OSRAM Accused Products, of which AMS-OSRAM TMF8828 is one example, are semiconductor devices.

Device Summary

Manufacturer	ams OSRAM
Foundry	Likely ams OSRAM
Part number	TMF8828
Type	FI d-ToF
Die thickness	150 µm
Die size, measured from the die edge	3.26 mm × 1.31 mm (4.3 mm^2)
Process type	FI CMOS ToF
Number of metal layers	6 Cu, 1 Al, 1 Al MIM capacitor bottom electrode and 1 Ta-based top electrode
Number of poly layers	1
Contacted logic gate pitch	240 nm (SRAM CGP 220 nm)
Minimum metal pitch logic	180 nm
Minimum metal pitch pixel array	170 nm
Process generation	65 nm
Features measured to determine process generation	Logic contacted gate pitch, and minimum metal pitch

TMF8828 Report at 6.

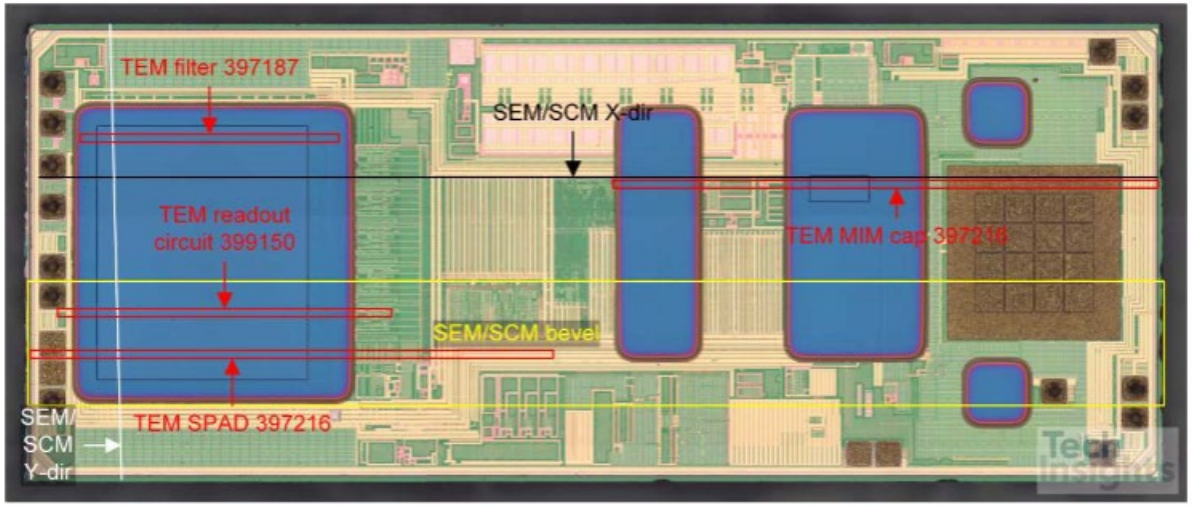
Annotated d-ToF Die Photograph at Substrate Level



ELZ-AN20_ToF_51084480_391407_Substrate.png

TMF8828 Report at 20.

Analysis Locations – SEM, SCM, and TEM

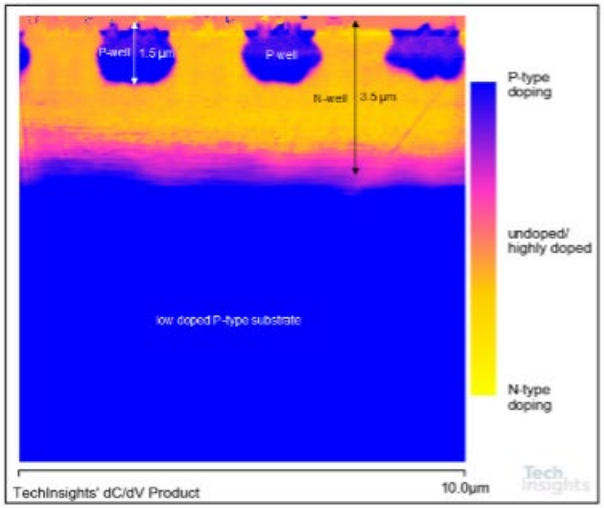


TMF8828_Analysis_Locations.png

TMF8828 Report at 21.

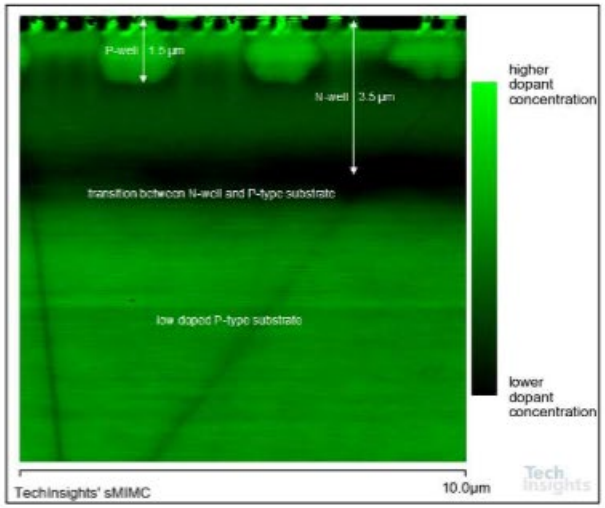
P- and N-Type Regions Logic – SPM

- SCM and SMIM-C cross section images in the logic region
- In the logic region, there is a 1.5 µm deep P-well, and a 3.5 µm deep N-well with a lower doped region at the bottom.
- The substrate is low doped P-type.



Logic_030922145952_PRODUCT_FRW_10.0u_512p_393092.png

Logic Region Wells – SCM

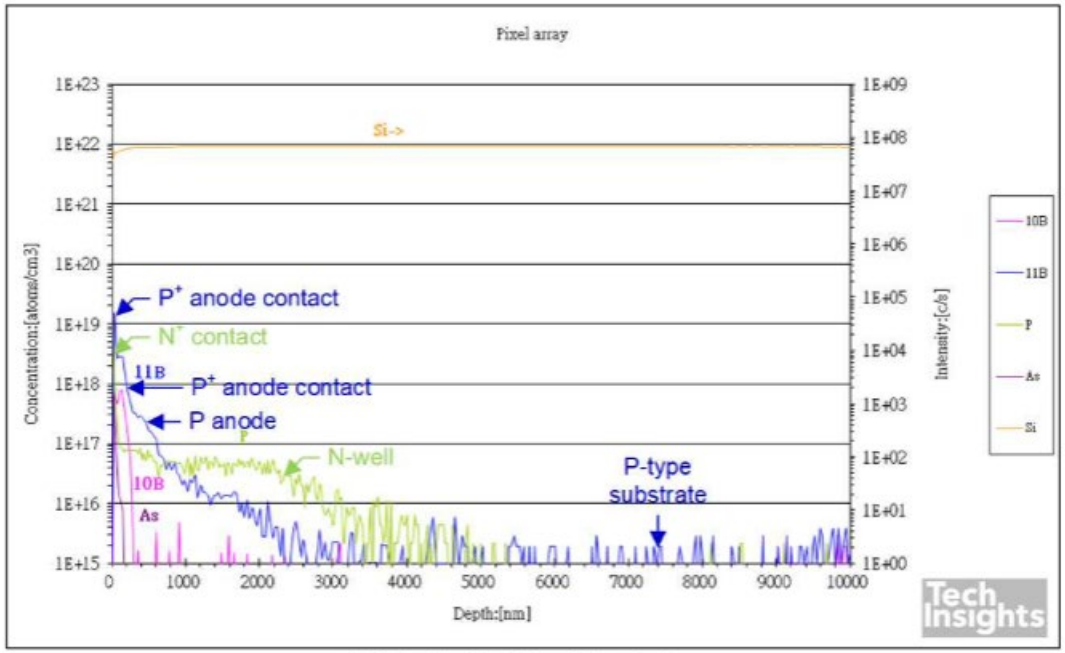


Logic_030922145952_SMIMC_FRW_10.0u_512p_393092.png

Logic Region Wells – SMIM-C

TMF8828 Report at 42.

P- and N-Type Doping Profiles SPAD Array – SIMS

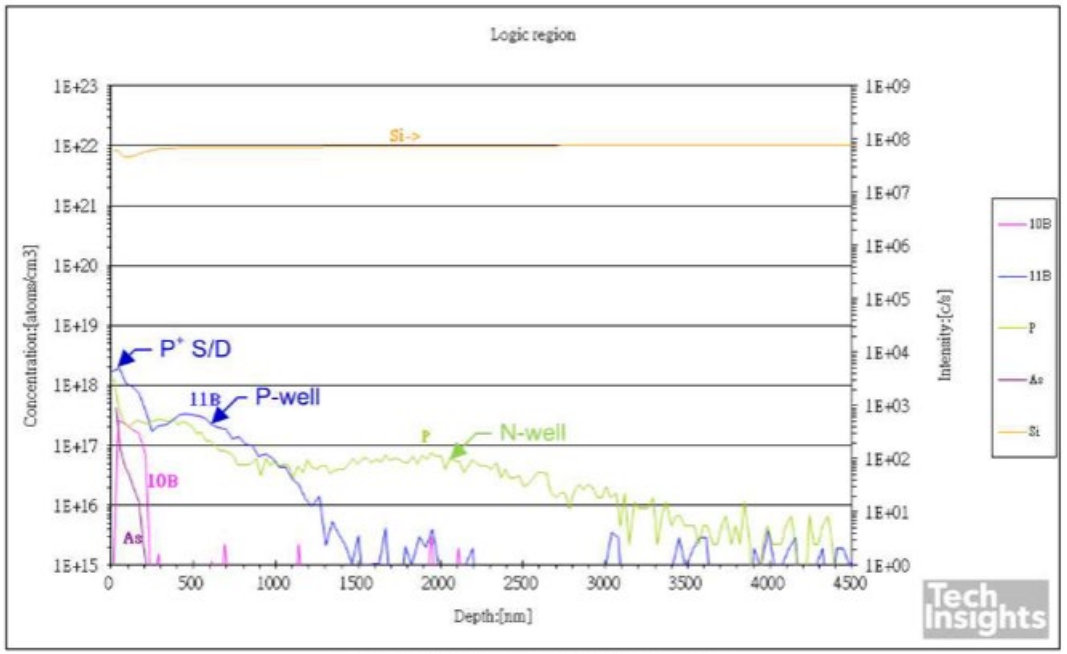


SIMS_Analysis_SPAD_Array_Doping_Profiles.png

SPAD Array Doping Profiles - SIMS

TMF8828 Report at 49.

P- and N-Type Doping Profiles Logic – SIMS



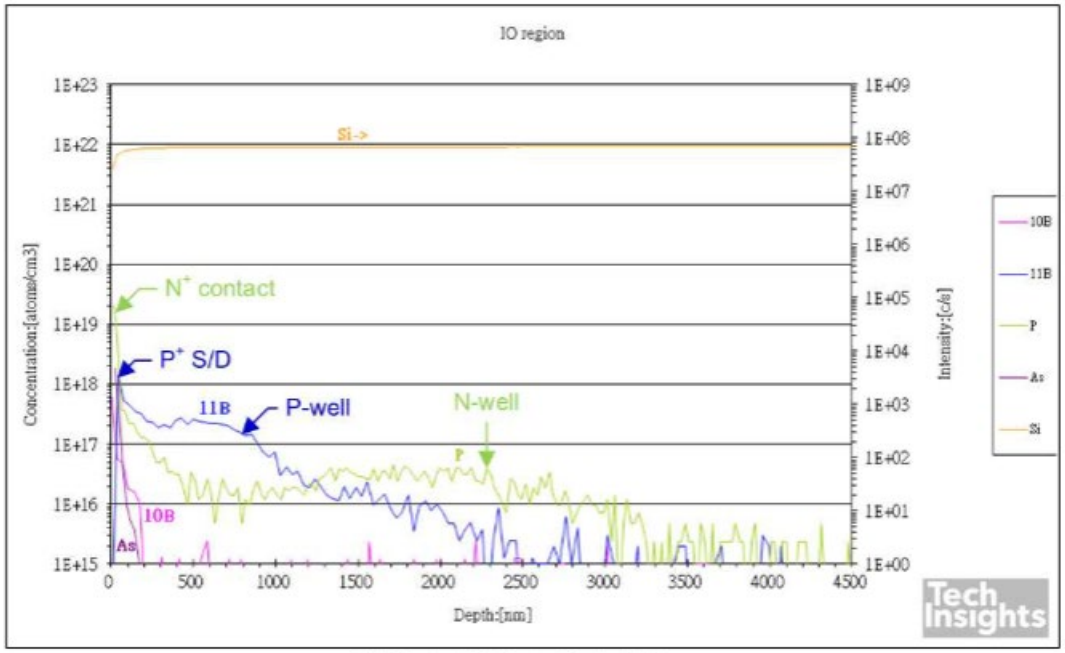
SIMS_Analysis_Logic_Region_Doping_Profiles.png

Logic Region Doping Profile – SIMS

51

TMF8828 Report at 51.

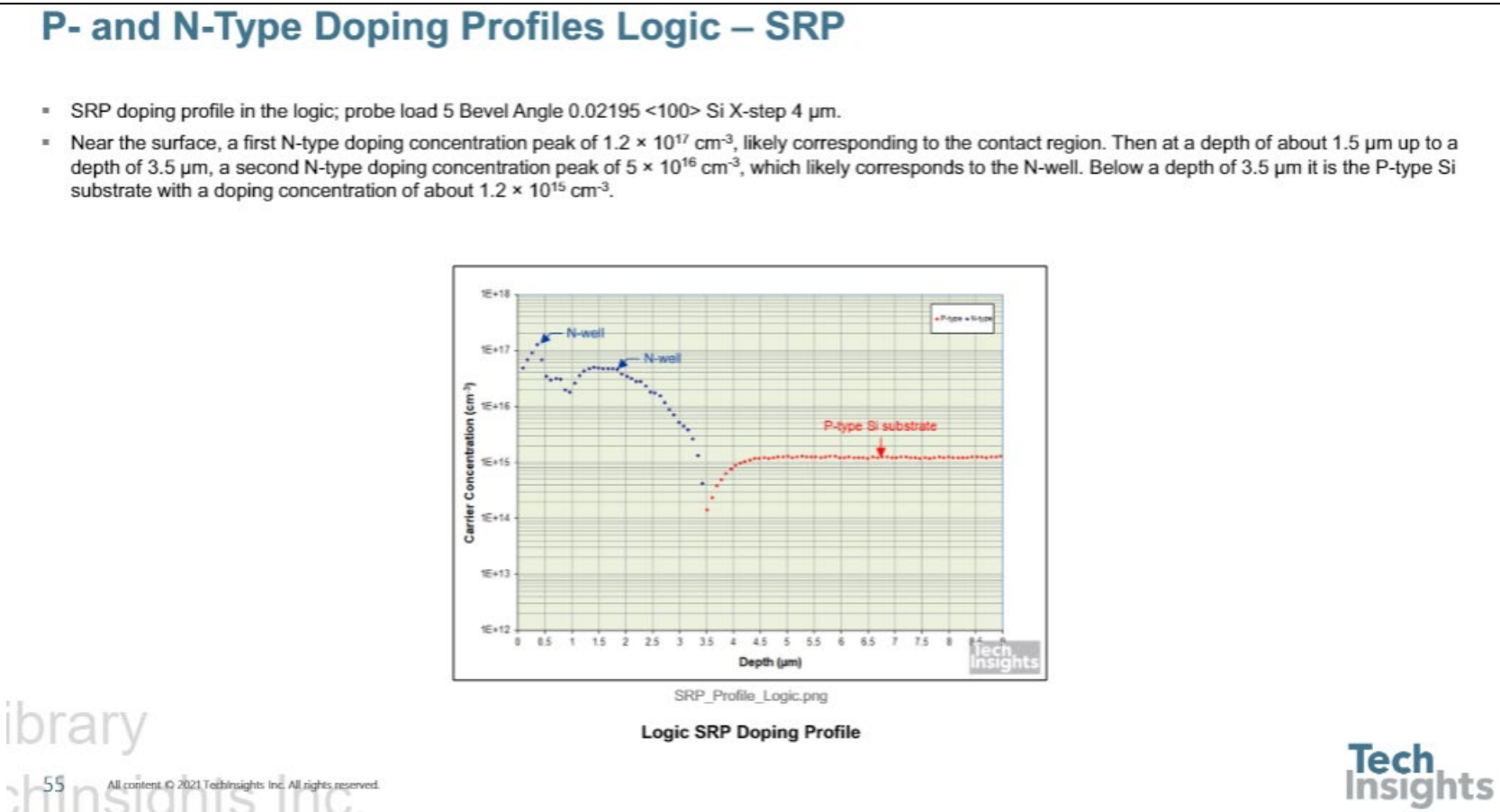
P- and N-Type Doping Profiles I/O – SIMS



SIMS_Analysis_IO_Region_Doping_Profiles.png

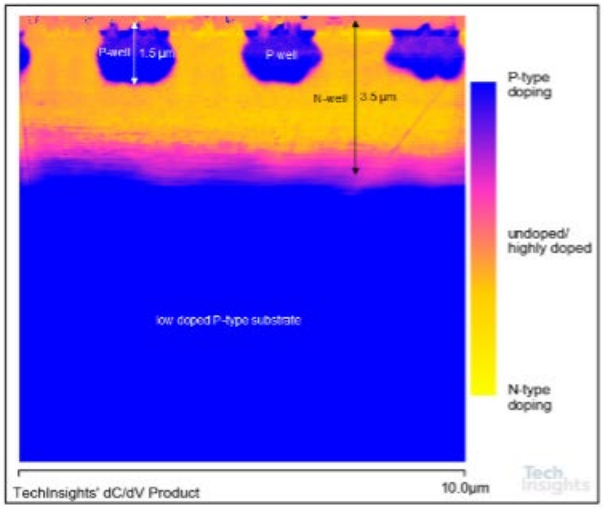
I/O Region Doping Profile – SIMS

TMF8828 Report at 53.

	 TMF8828 Report at 55.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The AMS-OSRAM Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary AMS-OSRAM Accused Product (the AMS-OSRAM TMF8828 discussed above) reveals the presence of such a substrate. For example, the AMS-OSRAM TMF8828 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. The SCM and sMIM-C images copied below show a P-type substrate having a first doping level, the substrate having a first and second surface. To the extent a second surface is not explicitly shown, on information and belief, the substrate will have a second surface below the first.

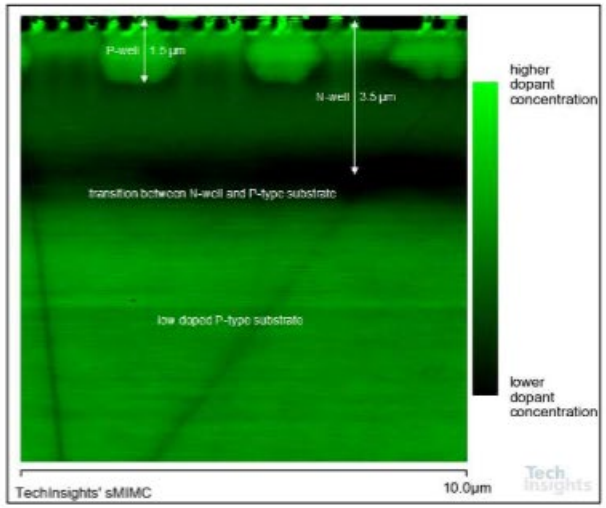
P- and N-Type Regions Logic – SPM

- SCM and SMIM-C cross section images in the logic region
- In the logic region, there is a 1.5 µm deep P-well, and a 3.5 µm deep N-well with a lower doped region at the bottom.
- The substrate is low doped P-type.



Logic_030922145952_PRODUCT_FRW_10.0u_512p_393092.png

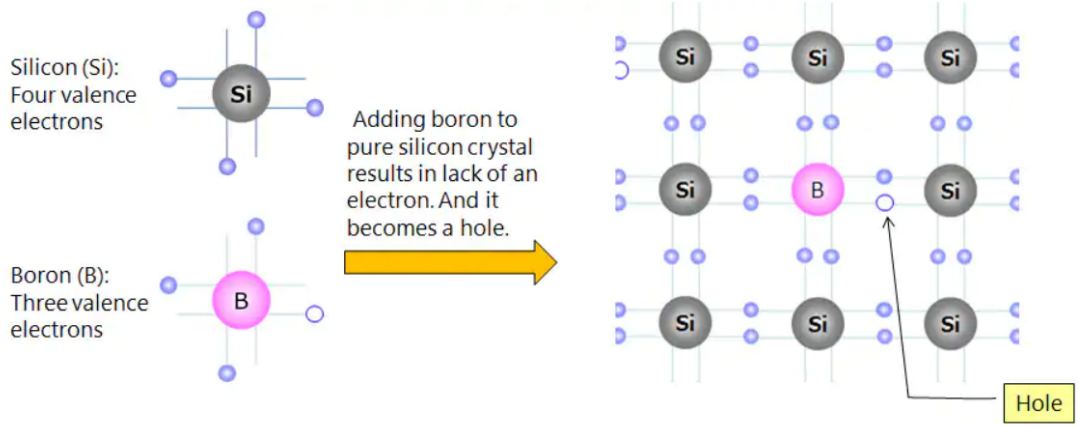
Logic Region Wells – SCM

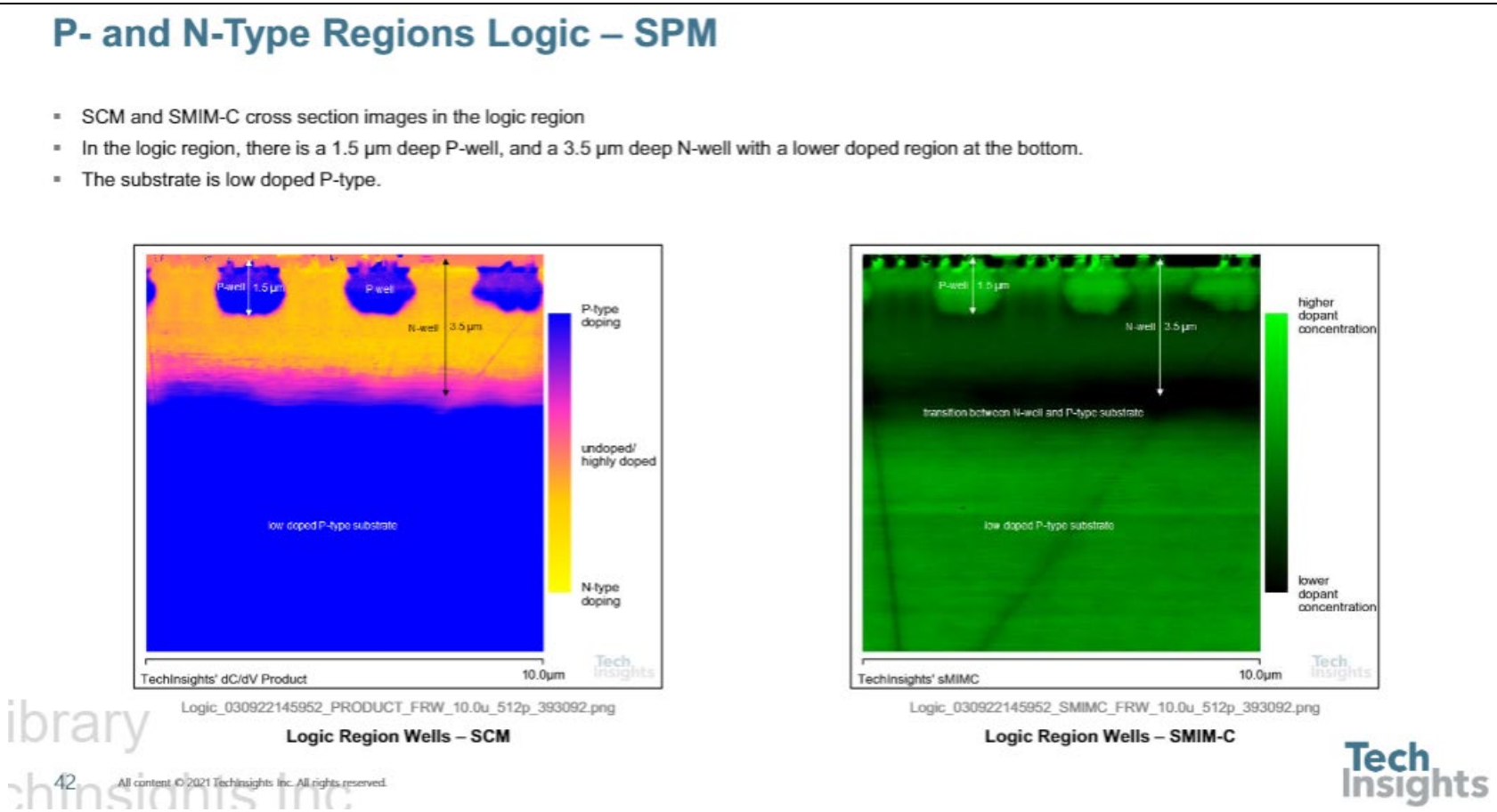


Logic_030922145952_SMIMC_FRW_10.0u_512p_393092.png

Logic Region Wells – SMIM-C

TMF8828 Report at 42.

	What is a p-type Semiconductor? A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "–" electrode in sequence.  * This hole is the carrier of a p-type semiconductor. *See* https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The AMS-OSRAM Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary AMS-OSRAM TMF8828 scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. See below showing "P- and N-Type Regions," where N-wells and P-wells are formed, the N-wells being disposed adjacent the first surface of the substrate with a second doping type (N-type doping) opposite in conductivity to the first doping type (P-type doping) and within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

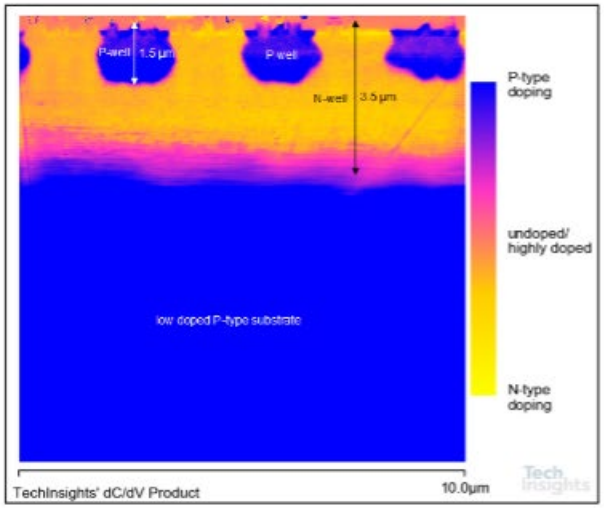
<table>
<tr>
<td></td>
<td>


TMF8828 Report at 42.
</td>
</tr>
<tr>
<td>[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and</td>
<td>The AMS-OSRAM Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the "P- and N-Type Regions Logic" reproduced at Claim 1, Element 2, shows where N-wells and P-wells are formed. The P-wells contain or comprise additional active regions separate from the first active regions contained or comprised by N-wells disposed adjacent to the first active region and within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.</td>
</tr>
</table>

within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The AMS-OSRAM Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at the "P- and N-Type Regions Logic" reproduced at Claim 1, Element 2, which shows where N-wells and P-wells are formed. This area represents a logic region where transistors are formed.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* above at Element 1. For example, this is shown by scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis, as well as the secondary ion mass spectroscopy (SIMS) analysis. Spreading resistance profiling (SRP) analysis shows a graded dopant concentration, as explained below. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from AMS-OSRAM Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the sMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. Further, the SIMS image shows doping concentration and doping type as a function of depth. The images below show vertical dopant grading in the active regions of the logic region. SRP and SIMS are well-known methods of studying semiconductor devices. *See e.g.*, T. Clarysse, et al. *Characterization of electrically active dopant profiles with the spreading resistance probe*, Materials Science and Engineering (December 2004). SRP provides an "electrical depth profile" and "gives intrinsically electrical information." Id. at 141, 157. Each SRP data point reflects carrier movement and dopant concentration at the physical location at which it was taken. The plots of SRP data taken from accused products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. That is the SRP plots included in Greenthread's infringement charts evidence both dopant gradients and the corresponding vertical electric drift fields. A silicon sample may be polished at an angle toward the top surface, and a defined profile may be generated over the depth of the sample via the grinding angle. The polished section was then electrically characterized using a step prober, which generated a depth profile. This graded dopant concentration aids carrier movement downward in the cross-sections shown below.

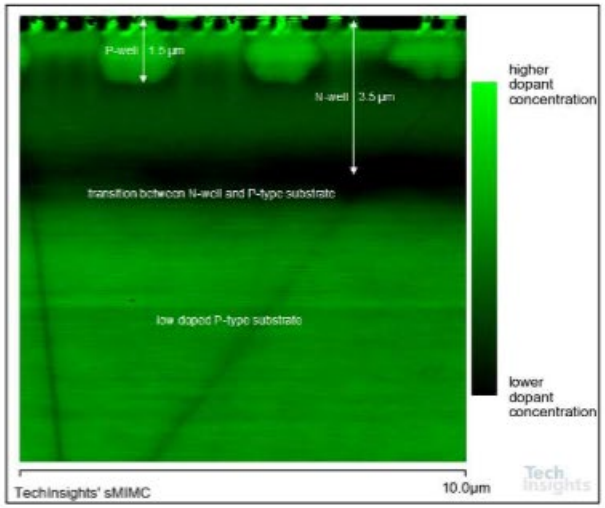
P- and N-Type Regions Logic – SPM

- SCM and SMIM-C cross section images in the logic region
- In the logic region, there is a 1.5 µm deep P-well, and a 3.5 µm deep N-well with a lower doped region at the bottom.
- The substrate is low doped P-type.



Logic_030922145952_PRODUCT_FRW_10.0u_512p_393092.png

Logic Region Wells – SCM

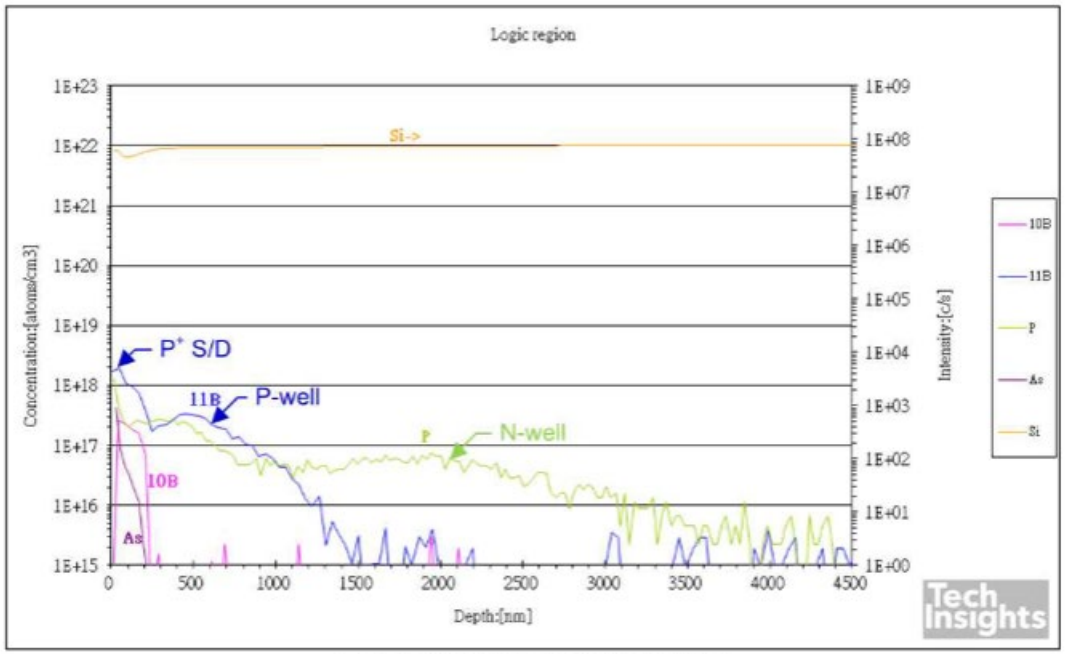


Logic_030922145952_SMIMC_FRW_10.0u_512p_393092.png

Logic Region Wells – SMIM-C

TMF8828 Report at 42.

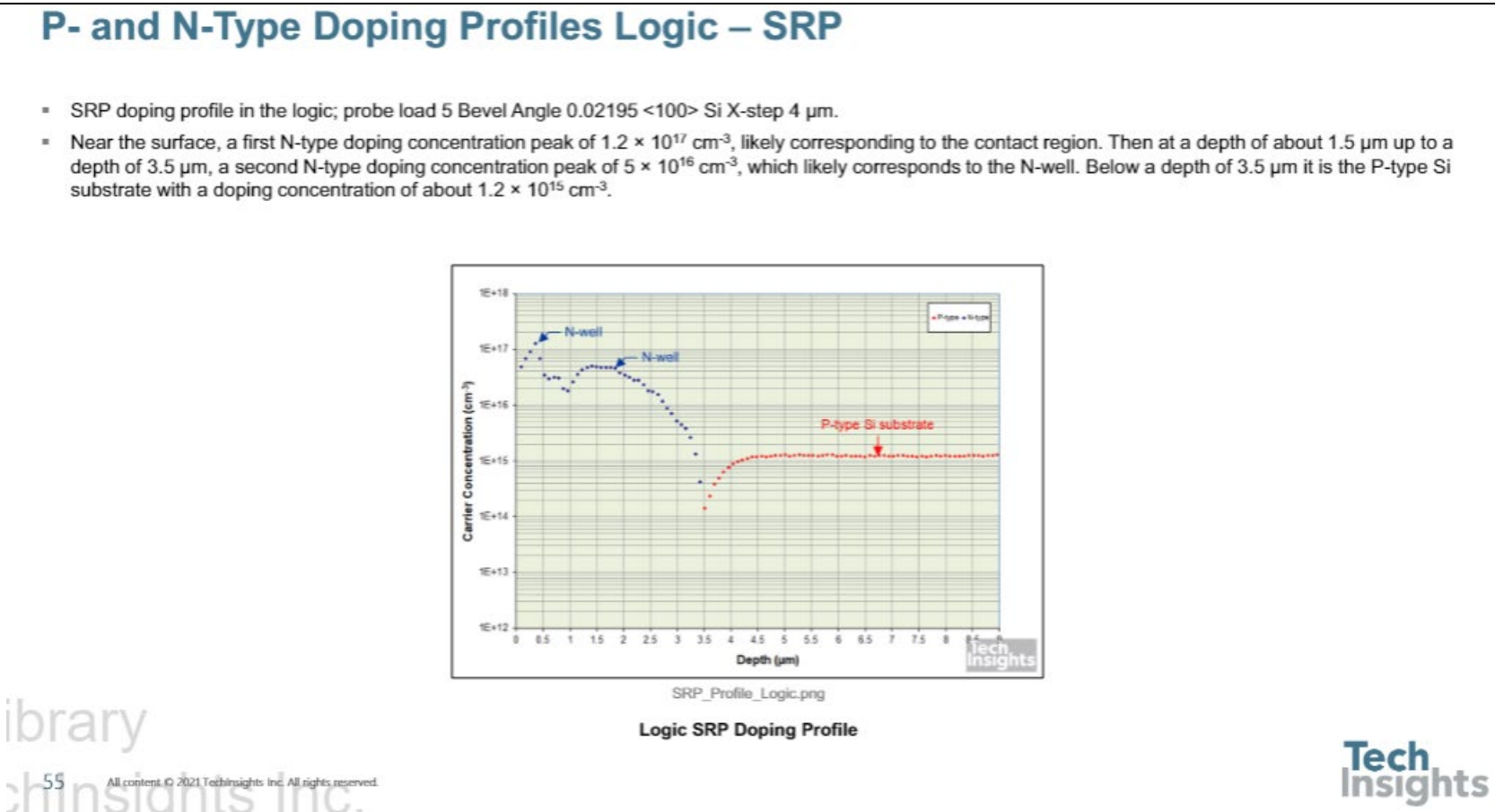
P- and N-Type Doping Profiles Logic – SIMS

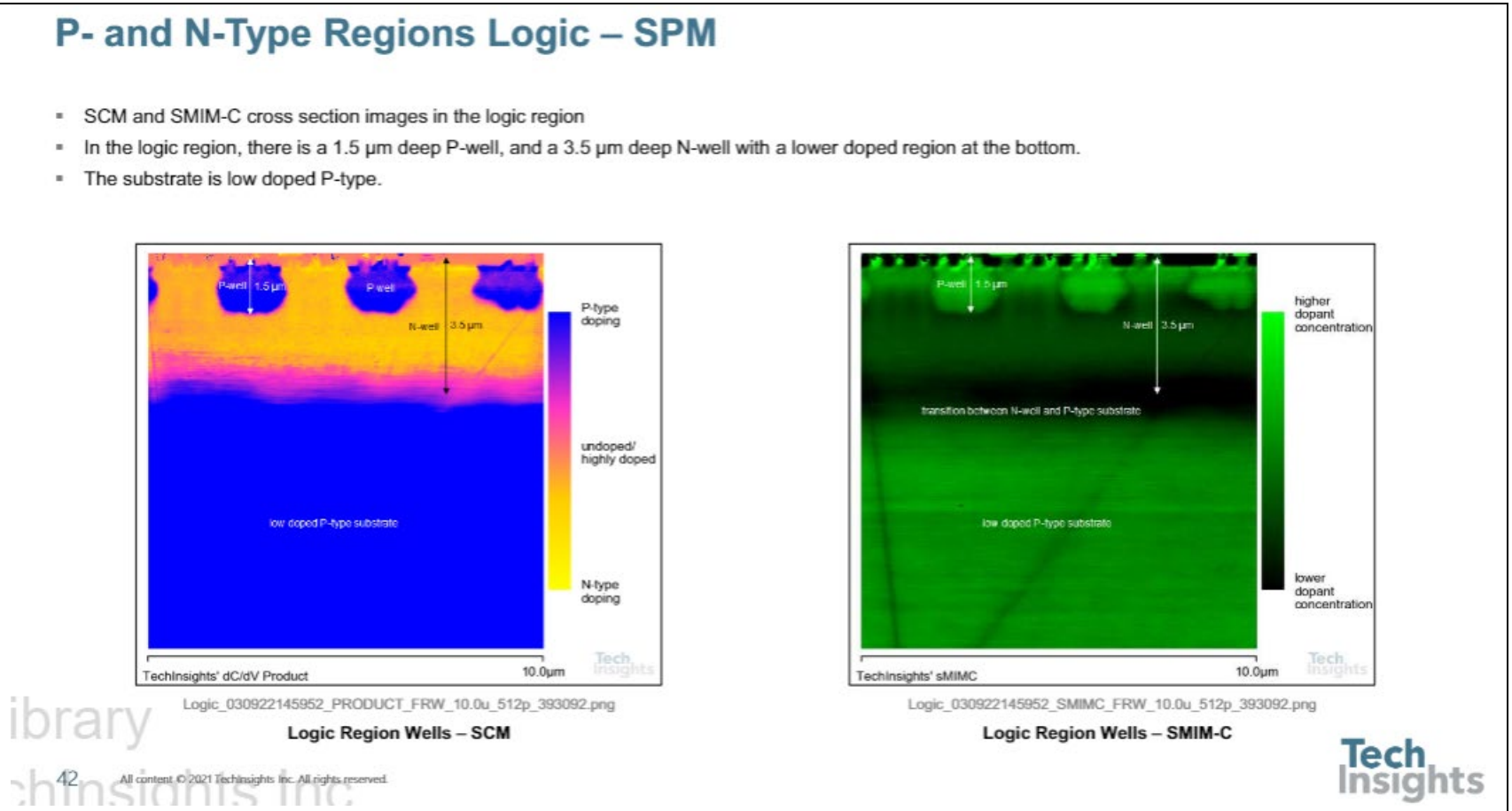


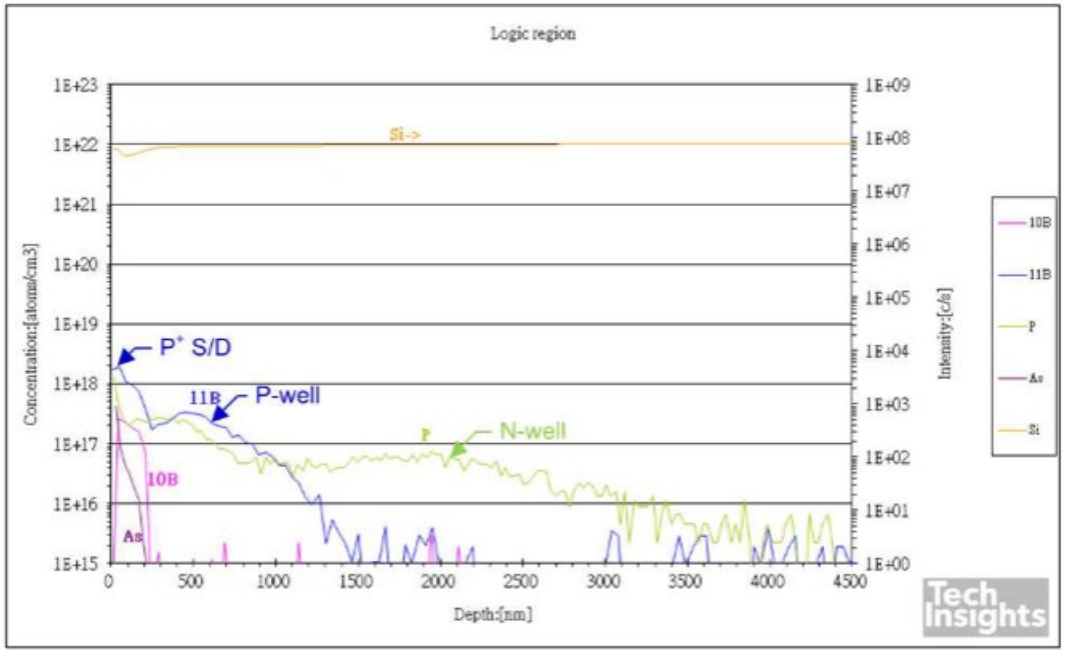
SIMS_Analysis_Logic_Region_Doping_Profiles.png

Logic Region Doping Profile – SIMS

TMF8828 Report at 51.

	 TMF8828 Report at 55.
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The AMS-OSRAM Accused Products meet this limitation. As shown in the image below, the substrate is a p-type substrate.

	 TMF8828 Report at 42.
4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	Upon information and belief, the substrate of the AMS-OSRAM Accused Products has epitaxial silicon on top of a nonepitaxial substrate. Epitaxial layers are well known in the industry. *See* https://www.powerwaywafer.com/why-do-semiconductor-devices-need-epitaxial-layer.html. Because it is well known in the art, the AMS-OSRAM Accused Products likely meet this limitation.
5. The semiconductor	The AMS-OSRAM Accused Products meet this limitation. As shown above, both N-well and P-wells are used in this device. The first and second active regions accordingly contain p-channel or n-channel devices. *See* Tech Insights Report images reproduced at Claim 1, Element 2.

device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The AMS-OSRAM Accused Products meet this limitation. As shown above, both N-well and P-wells are used in the logic region of this device. The first and second active regions accordingly contain p-channel or n-channel devices. *See* Tech Insights Report images reproduced at Claim 1, Element 2. Each well has a graded dopant, as shown below. **P- and N-Type Doping Profiles Logic – SIMS**  SIMS_Analysis_Logic_Region_Doping_Profiles.png **Logic Region Doping Profile – SIMS** 51 TMF8828 Report at 51.

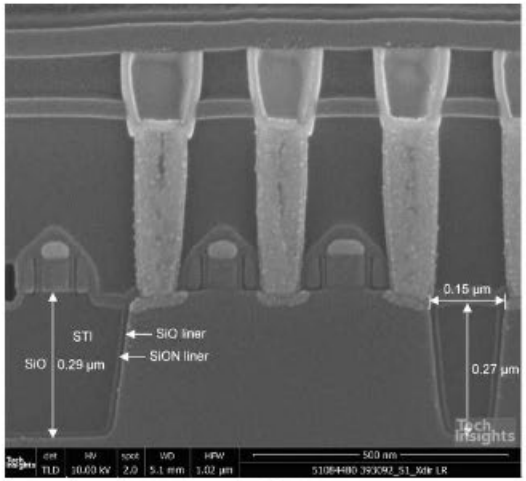
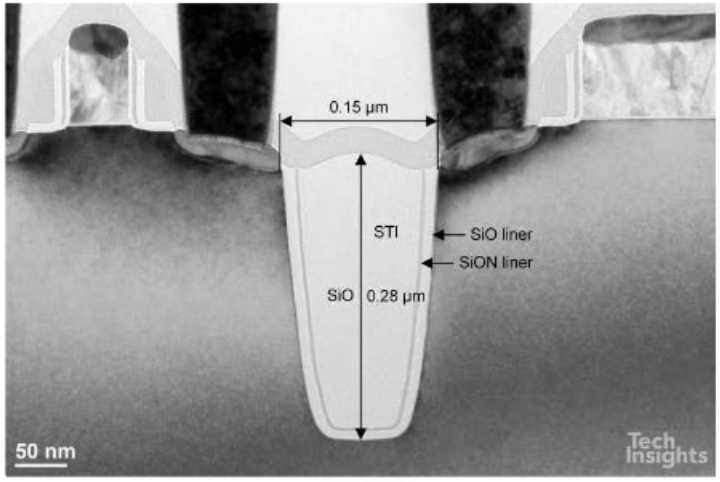
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the substrate of the AMS-OSRAM Accused Products have isolation regions that separate the first and second active regions. As shown below, SEM and TEM cross section images show the use of at least one isolation region (annotated as STI) in the logic region. **Isolation – STI** ▪ SEM and TEM cross section images of the STI in the logic region. The STI in the logic and other regions of the die is the same. ▪ In the logic region the STI is 0.27-0.28 µm thick under the CESL nitride and 0.29 µm thick under the polysilicon. ▪ The STI is lined with oxide and SiON and filled with oxide.  588_Peripheral_MOS_393092.png **Logic Region STI – SEM**  sti 35k_397216.png **Logic Region STI – TEM** brary 58 All content © 2021 Techinsights Inc. All rights reserved. chinsights Inc. TMF8828 Report at 58.
8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the AMS-OSRAM Accused Products. Information about the fabrication process for the AMS-OSRAM Accused Products, including usage of an ion implantation process, is in the possession of Defendants and is expected to be obtained through discovery.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

implantation process.	
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 2.
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 3.

first active region and within which transistors can be formed in the surface thereof;	
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 5.
10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 2.
12. The semiconductor device of claim 9, wherein the substrate has	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 4.

epitaxial silicon on top of a nonepitaxial substrate.	
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 5.
14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 6.
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at	Upon information and belief, the AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 7.

least one isolation region.	
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	The AMS-OSRAM Accused Products meet this limitation. As discussed above for Claim 1, the AMS-OSRAM Accused Products include first and second active regions. Upon information and belief, CMOS transistors are formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendants and are expected to be obtained through discovery.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

U.S. Patent No. 10,734,481	Exemplary Accused Product AMS-OSRAM TMF8828 configurable 8x8 multi-zone Time-of-Flight Sensor
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a semiconductor device. This chart includes exemplary information regarding a representative example of the AMS-OSRAM Accused Products, the AMS-OSRAM TMF8828 ("TMF8828"). The TMF8828 was analyzed in the below-referenced report from Tech Insights. The complete report is hereby incorporated by reference into each and every claim and claim element discussed. "AMS-OSRAM TMF8828, 17 µm × 39 µm Pixel Pitch d-ToF Sensor from Honor Magic3 Pro Rear-Facing Camera Device Essentials Plus Summary," *available at* https://library.techinsights.com/search/device-details?tab=reports&id=DEP-2110-801&genealogyCode=HNR-ELZ-AN10_ToF&activeTab=Reports ("TMF8828 Report"). Selected pages are reproduced herein to aid in understanding. Tech Insights techinsights.com ams OSRAM TMF8828, 17 µm × 39 µm Pixel Pitch d-ToF Sensor from Honor Magic3 Pro Rear-Facing Camera Device Essentials Plus Summary TMF8828 Report at Cover. The AMS-OSRAM TMF8828 is representative of the AMS-OSRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other AMS-OSRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, the other AMS-OSRAM Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Similarly, the other AMS-OSRAM Accused Products would have been designed in a similar manner as the AMS-OSRAM TMF8828 for purposes of this claim chart to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828 transistors depicted here, and function in a

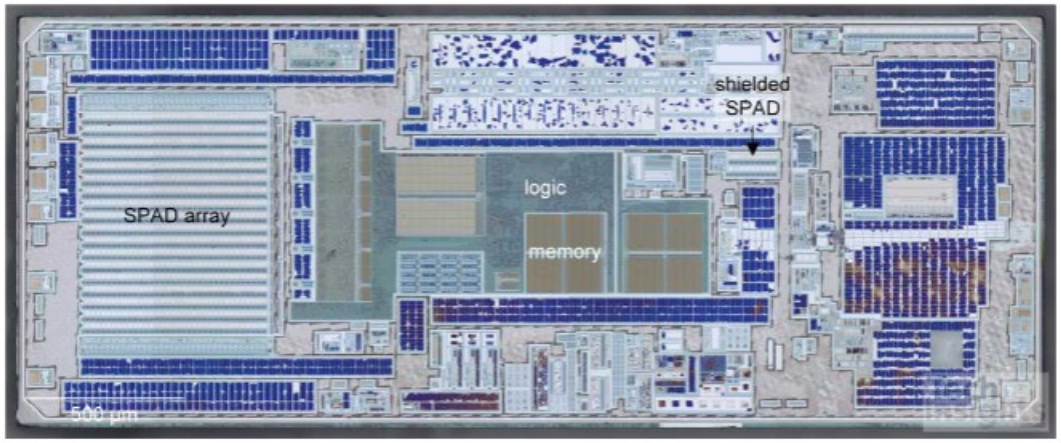
similar way with respect to the features claimed in the asserted claims, and the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828, and function in a similar way with respect to the features claimed in the asserted claims.

This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The AMS-OSRAM Accused Products, of which AMS-OSRAM TMF8828 is one example, are semiconductor devices.

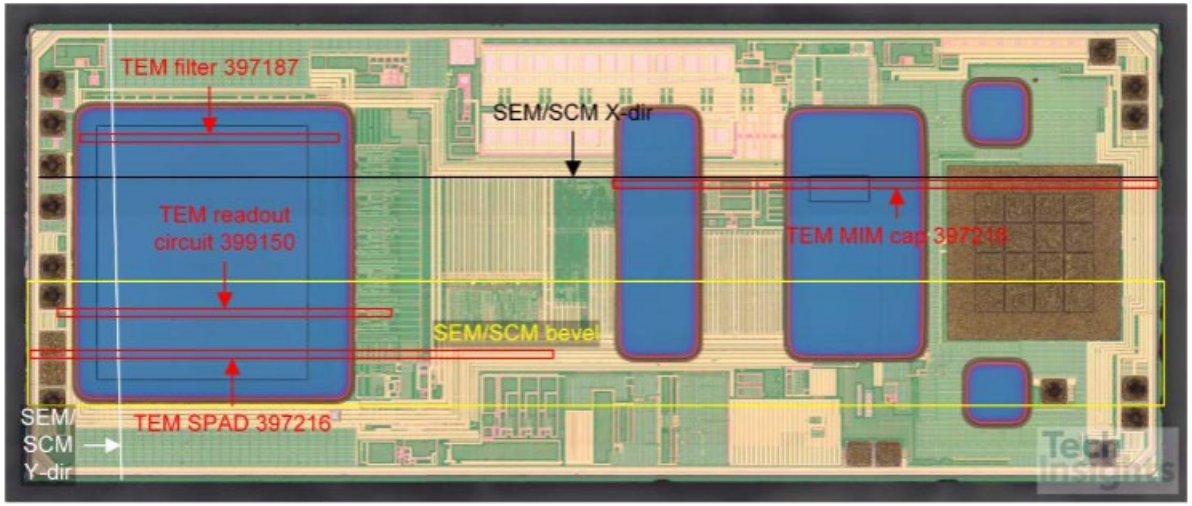
Device Summary

Manufacturer	ams OSRAM
Foundry	Likely ams OSRAM
Part number	TMF8828
Type	FI d-ToF
Die thickness	150 µm
Die size, measured from the die edge	3.26 mm × 1.31 mm (4.3 mm^2)
Process type	FI CMOS ToF
Number of metal layers	6 Cu, 1 Al, 1 Al MIM capacitor bottom electrode and 1 Ta-based top electrode
Number of poly layers	1
Contacted logic gate pitch	240 nm (SRAM CGP 220 nm)
Minimum metal pitch logic	180 nm
Minimum metal pitch pixel array	170 nm
Process generation	65 nm
Features measured to determine process generation	Logic contacted gate pitch, and minimum metal pitch

TMF8828 Report at 6.

	Annotated d-ToF Die Photograph at Substrate Level  ELZ-AN20_ToF_51084480_391407_Substrate.png TMF8828 Report at 20.

Analysis Locations – SEM, SCM, and TEM

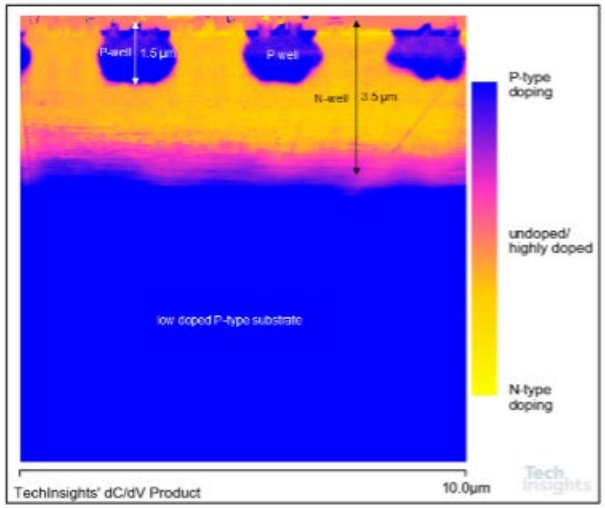


TMF8828_Analysis_Locations.png

TMF8828 Report at 21.

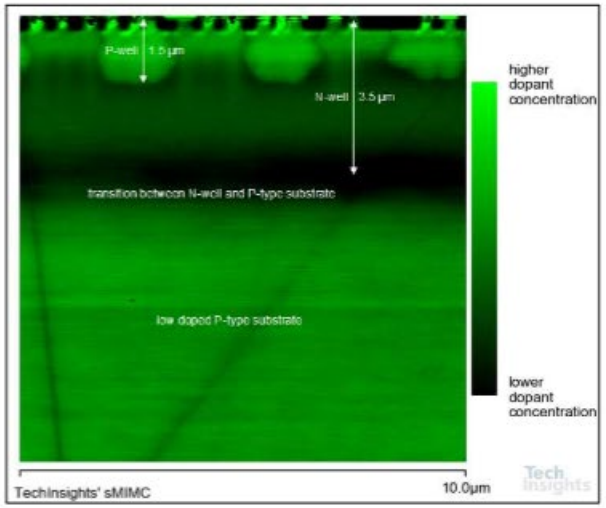
P- and N-Type Regions Logic – SPM

- SCM and SMIM-C cross section images in the logic region
- In the logic region, there is a 1.5 µm deep P-well, and a 3.5 µm deep N-well with a lower doped region at the bottom.
- The substrate is low doped P-type.



Logic_030922145952_PRODUCT_FRW_10.0u_512p_393092.png

Logic Region Wells – SCM

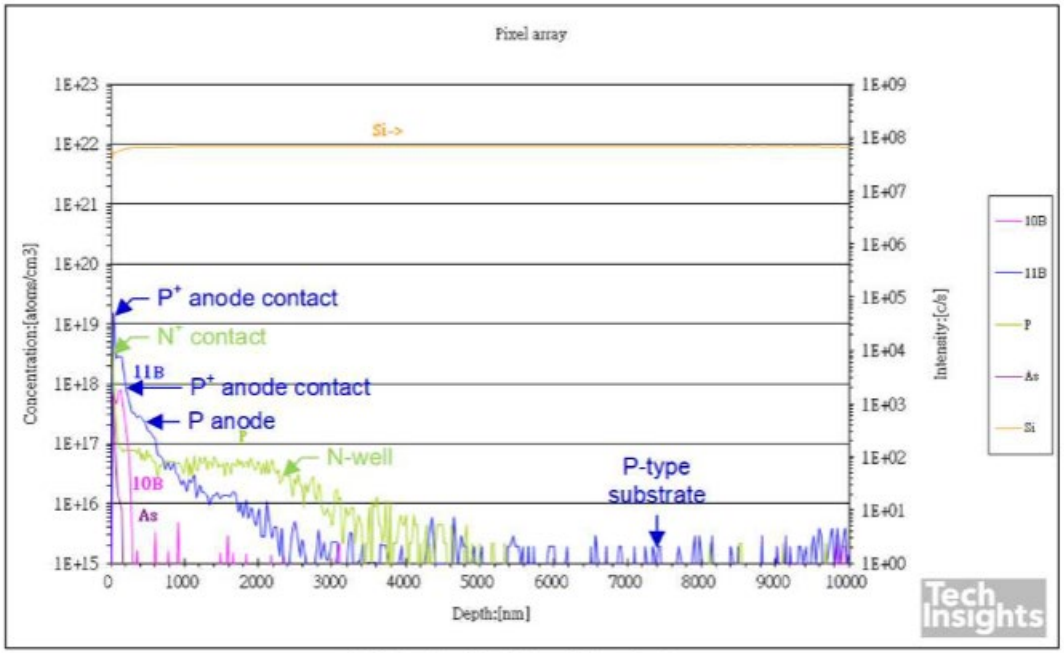


Logic_030922145952_SMIMC_FRW_10.0u_512p_393092.png

Logic Region Wells – SMIM-C

TMF8828 Report at 42.

P- and N-Type Doping Profiles SPAD Array – SIMS



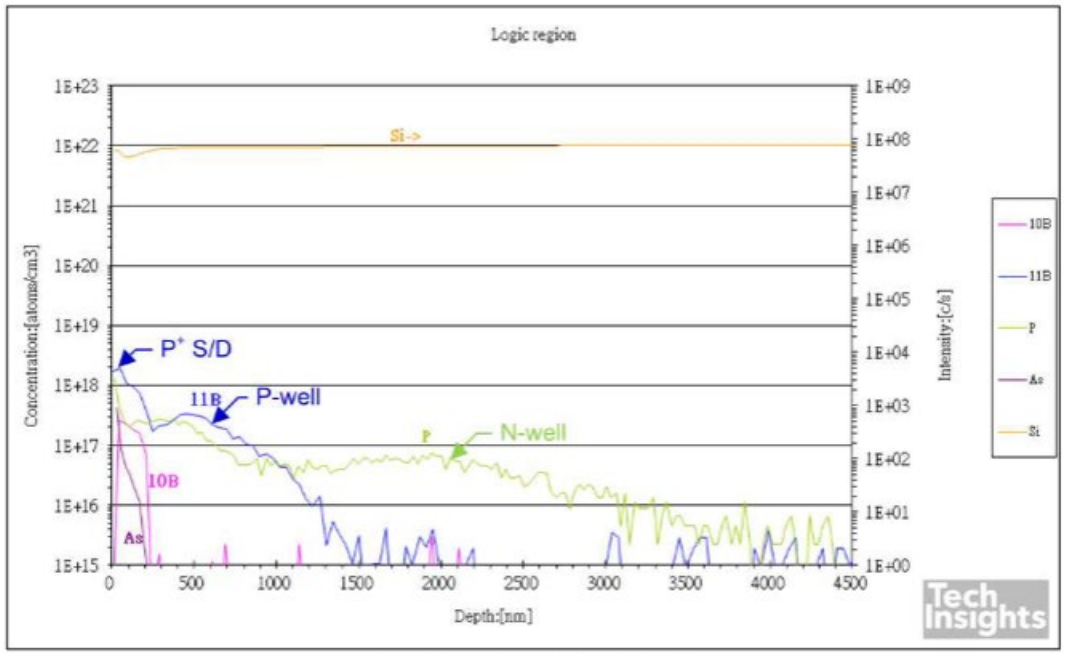
SIMS_Analysis_SPAD_Array_Doping_Profiles.png

SPAD Array Doping Profiles - SIMS

49

TMF8828 Report at 49.

P- and N-Type Doping Profiles Logic – SIMS



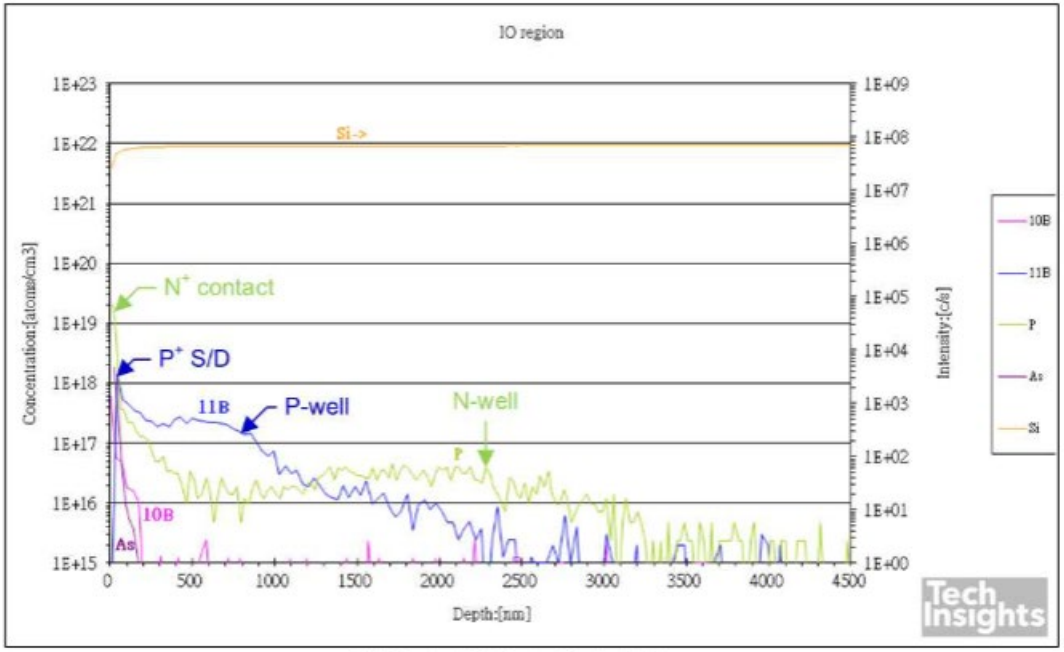
SIMS_Analysis_Logic_Region_Doping_Profiles.png

Logic Region Doping Profile – SIMS

51

TMF8828 Report at 51.

P- and N-Type Doping Profiles I/O – SIMS

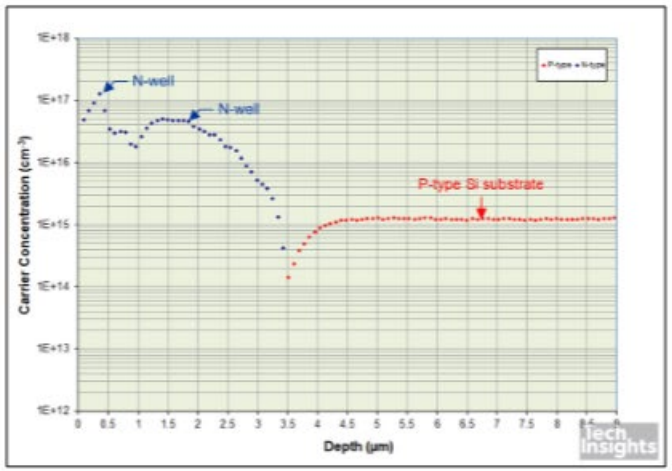


SIMS_Analysis_IO_Region_Doping_Profiles.png

I/O Region Doping Profile – SIMS

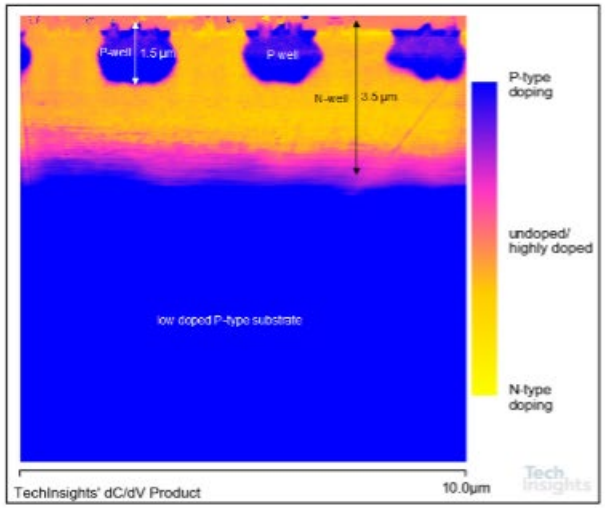
53

TMF8828 Report at 53.

	P- and N-Type Doping Profiles Logic – SRP ▪ SRP doping profile in the logic; probe load 5 Bevel Angle 0.02195 <100> Si X-step 4 µm. ▪ Near the surface, a first N-type doping concentration peak of 1.2×10^{17} cm^{-3}, likely corresponding to the contact region. Then at a depth of about 1.5 µm up to a depth of 3.5 µm, a second N-type doping concentration peak of 5×10^{16} cm^{-3}, which likely corresponds to the N-well. Below a depth of 3.5 µm it is the P-type Si substrate with a doping concentration of about 1.2×10^{15} cm^{-3}.  SRP_Profile_Logic.png **Logic SRP Doping Profile** TMF8828 Report at 55.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The AMS-OSRAM Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary AMS-OSRAM Accused Product (the AMS-OSRAM TMF8828 discussed above) reveals the presence of such a substrate. For example, the AMS-OSRAM TMF8828 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. The SCM image of the logic region shows a P-type substrate having a first doping level, the substrate having a first and second surface. To the extent a second surface is not explicitly shown, on information and belief, the substrate will have a second surface below the first.

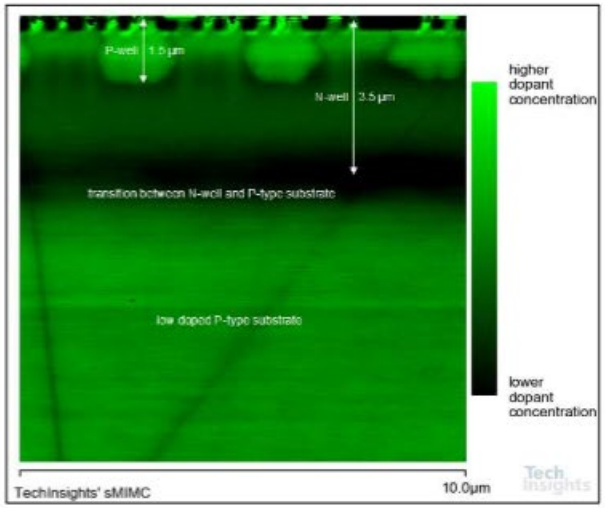
P- and N-Type Regions Logic – SPM

- SCM and SMIM-C cross section images in the logic region
- In the logic region, there is a 1.5 µm deep P-well, and a 3.5 µm deep N-well with a lower doped region at the bottom.
- The substrate is low doped P-type.



Logic_030922145952_PRODUCT_FRW_10.0u_512p_393092.png

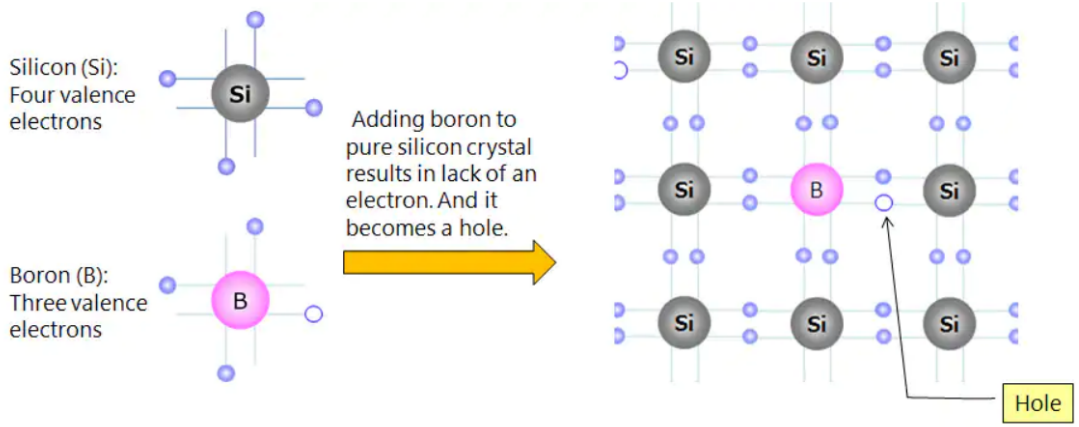
Logic Region Wells – SCM

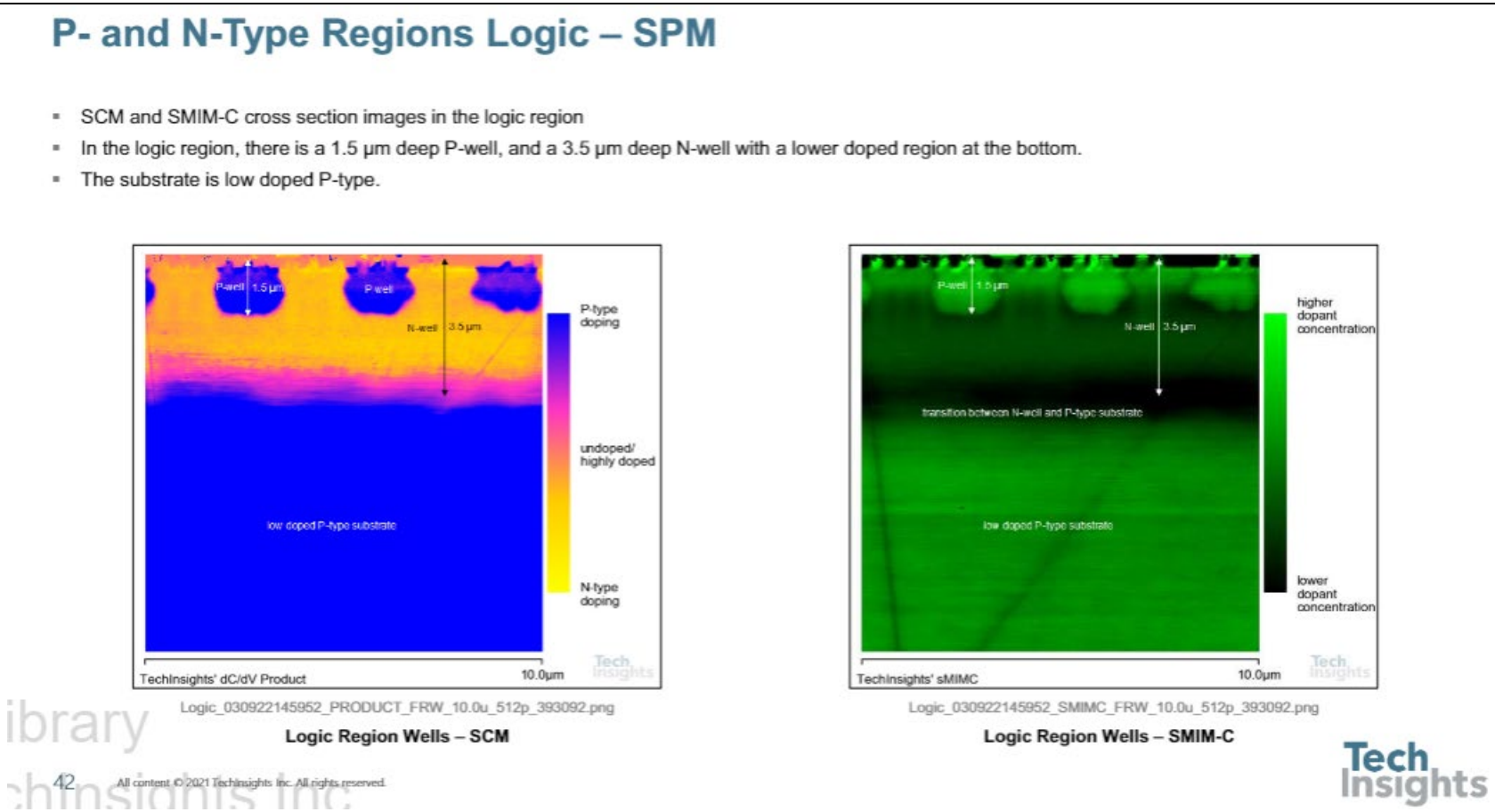


Logic_030922145952_SMIMC_FRW_10.0u_512p_393092.png

Logic Region Wells – SMIM-C

TMF8828 Report at 42.

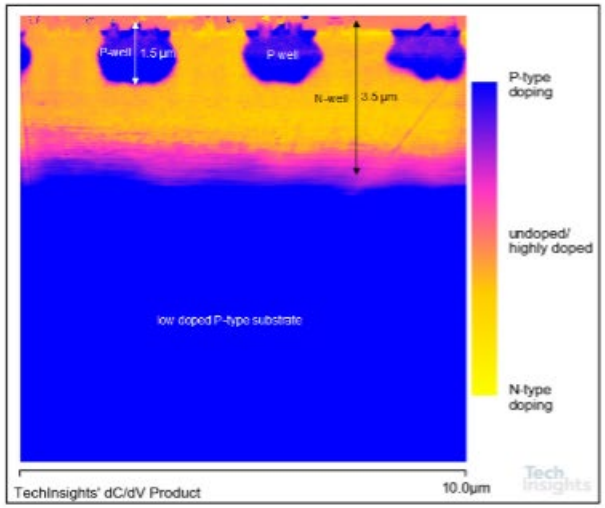
	What is a p-type Semiconductor? A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "–" electrode in sequence.  * This hole is the carrier of a p-type semiconductor. *See* https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The AMS-OSRAM Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary AMS-OSRAM TMF8828 scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. See below showing "P- and N-Type Regions Logic," where N-wells and P-wells are formed, the N-wells being disposed adjacent the first surface of the substrate with a second doping type (N-type doping) opposite in conductivity to the first doping type (P-type doping) and within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

	 TMF8828 Report at 42.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and	The AMS-OSRAM Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the "P- and N-Type Regions Logic" reproduced at Claim 1, Element 2, which shows where N-wells and P-wells are formed. The P-wells contain or comprise additional active regions separate from the first active regions contained or comprised by N-wells disposed adjacent to the first active region and within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The AMS-OSRAM Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at the "P- and N-Type Regions Logic" reproduced at Claim 1, Element 2, which shows where N-wells and P-wells are formed. This area represents a logic region where transistors are formed.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The AMS-OSRAM Accused Products meet this limitation. *See* above at Element 1. For example, this is shown by scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis, as well as the secondary ion mass spectroscopy (SIMS) analysis. Spreading resistance profiling (SRP) analysis shows a graded dopant concentration, as explained below. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from AMS-OSRAM Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the sMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. Further, the SIMS image shows doping concentration and doping type as a function of depth. The images below show vertical dopant grading in the active regions of the logic region. SRP and SIMS are well-known methods of studying semiconductor devices. *See e.g.*, T. Clarysse, et al. *Characterization of electrically active dopant profiles with the spreading resistance probe*, Materials Science and Engineering (December 2004). SRP provides an "electrical depth profile" and "gives intrinsically electrical information." Id. at 141, 157. Each SRP data point reflects carrier movement and dopant concentration at the physical location at which it was taken. The plots of SRP data taken from accused products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. That is the SRP plots included in Greenthread's infringement charts evidence both dopant gradients and the corresponding vertical electric drift fields. A silicon sample may be polished at an angle toward the top surface, and a defined profile may be generated over the depth of the sample via the grinding angle. The polished section was then electrically characterized using a step prober, which generated a depth profile. This graded dopant concentration aids carrier movement downward in the cross-sections shown below.

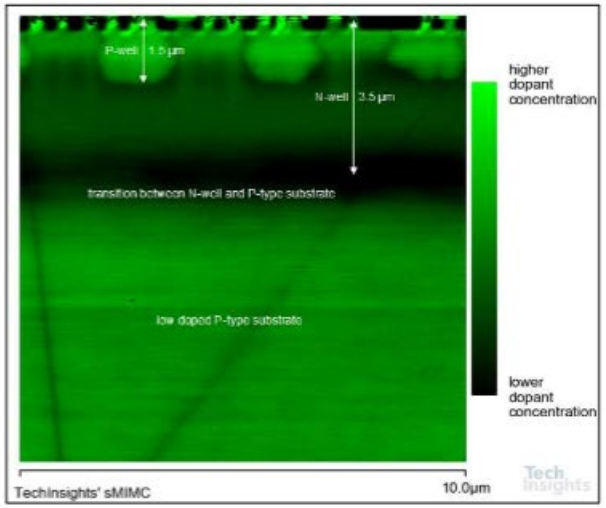
P- and N-Type Regions Logic – SPM

- SCM and SMIM-C cross section images in the logic region
- In the logic region, there is a 1.5 µm deep P-well, and a 3.5 µm deep N-well with a lower doped region at the bottom.
- The substrate is low doped P-type.



Logic_030922145952_PRODUCT_FRW_10.0u_512p_393092.png

Logic Region Wells – SCM

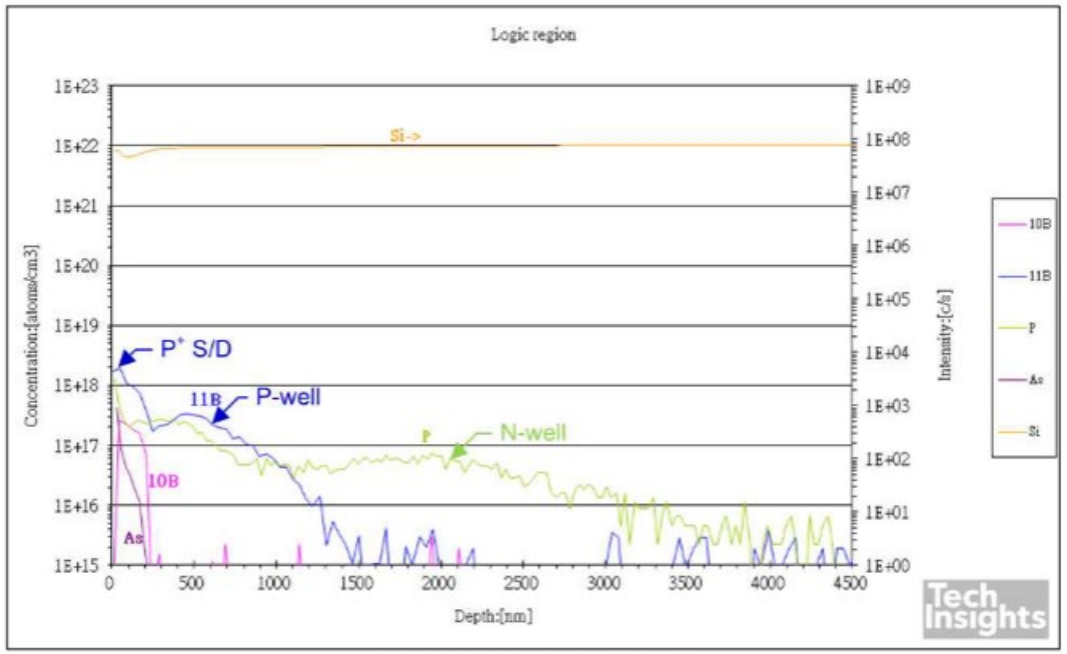


Logic_030922145952_SMIMC_FRW_10.0u_512p_393092.png

Logic Region Wells – SMIM-C

TMF8828 Report at 42.

P- and N-Type Doping Profiles Logic – SIMS



SIMS_Analysis_Logic_Region_Doping_Profiles.png

Logic Region Doping Profile – SIMS

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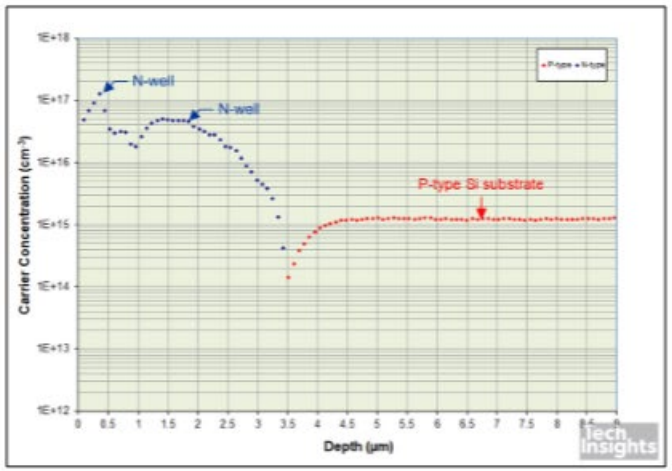
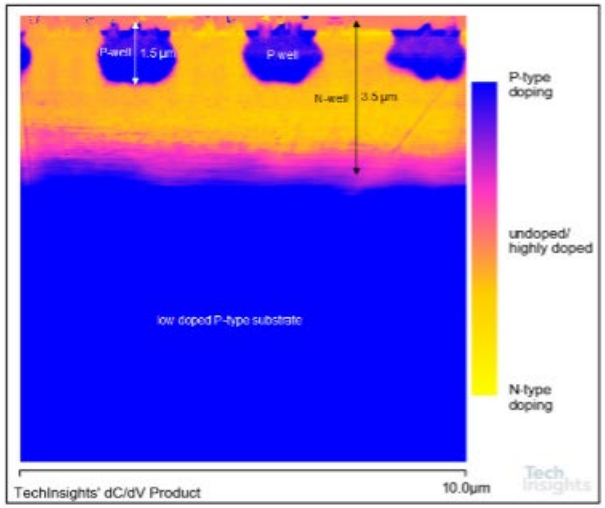
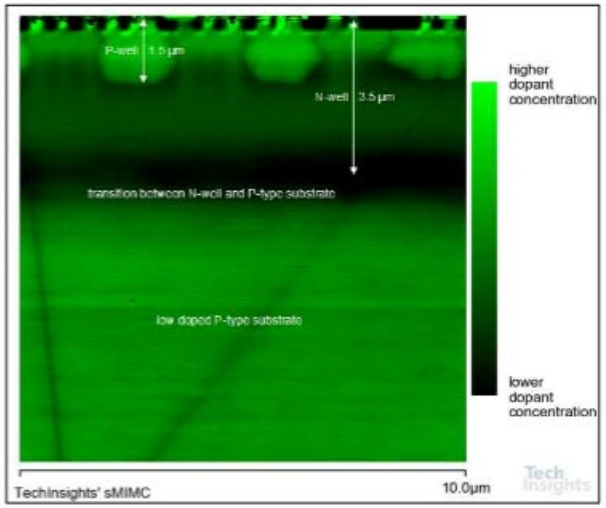
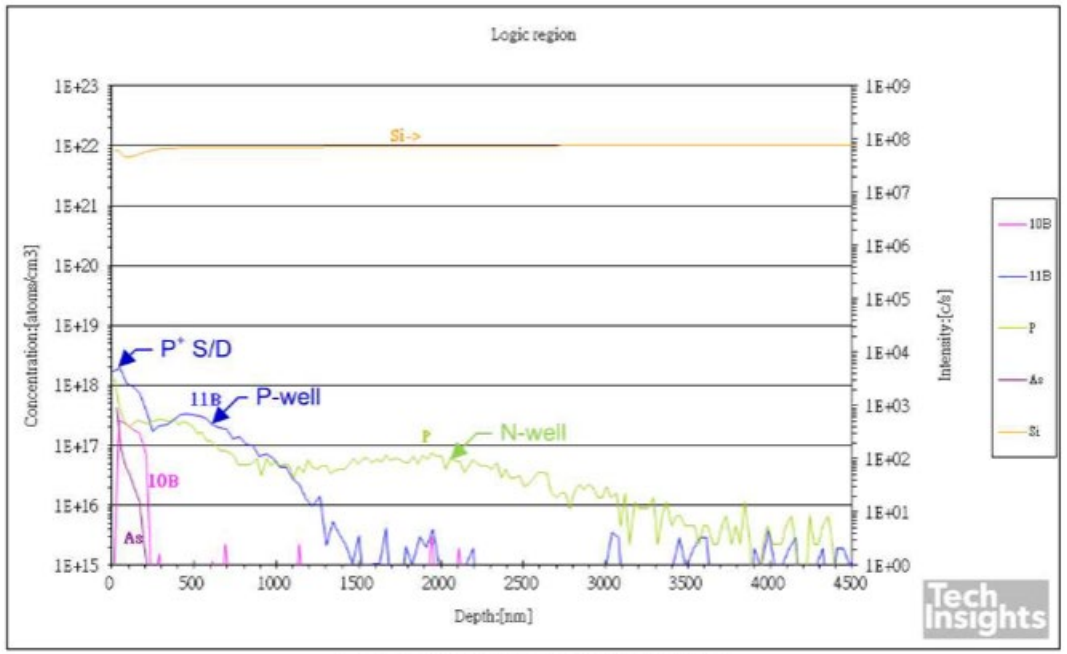
TMF8828 Report at 51.

	P- and N-Type Doping Profiles Logic – SRP ▪ SRP doping profile in the logic; probe load 5 Bevel Angle 0.02195 <100> Si X-step 4 µm. ▪ Near the surface, a first N-type doping concentration peak of 1.2×10^{17} cm^{-3}, likely corresponding to the contact region. Then at a depth of about 1.5 µm up to a depth of 3.5 µm, a second N-type doping concentration peak of 5×10^{16} cm^{-3}, which likely corresponds to the N-well. Below a depth of 3.5 µm it is the P-type Si substrate with a doping concentration of about 1.2×10^{15} cm^{-3}.  SRP_Profile_Logic.png **Logic SRP Doping Profile** TMF8828 Report at 55.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region,	The AMS-OSRAM Accused Products meet this limitation. *See* above at Element 1. For example, this is shown by the SIMS and scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis, as well as the spreading resistance profiling (SRP) analysis. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from AMS-OSRAM Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the sMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. Further, SRP is a technique used to analyze resistivity versus depth in semiconductors, and the SRP images show doping concentration and doping type as a function of depth. The images below show vertical dopant grading in the active regions of the logic region. The image below shows vertical

the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	dopant grading in a well region adjacent (N-well and P-well) to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate. **P- and N-Type Regions Logic – SPM** ▪ SCM and SMIM-C cross section images in the logic region ▪ In the logic region, there is a 1.5 µm deep P-well, and a 3.5 µm deep N-well with a lower doped region at the bottom. ▪ The substrate is low doped P-type.  Logic_030922145952_PRODUCT_FRW_10.0u_512p_393092.png **Logic Region Wells – SCM**  Logic_030922145952_SMIMC_FRW_10.0u_512p_393092.png **Logic Region Wells – SMIM-C** 42 TMF8828 Report at 42.

P- and N-Type Doping Profiles Logic – SIMS



SIMS_Analysis_Logic_Region_Doping_Profiles.png

Logic Region Doping Profile – SIMS

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TMF8828 Report at 51.

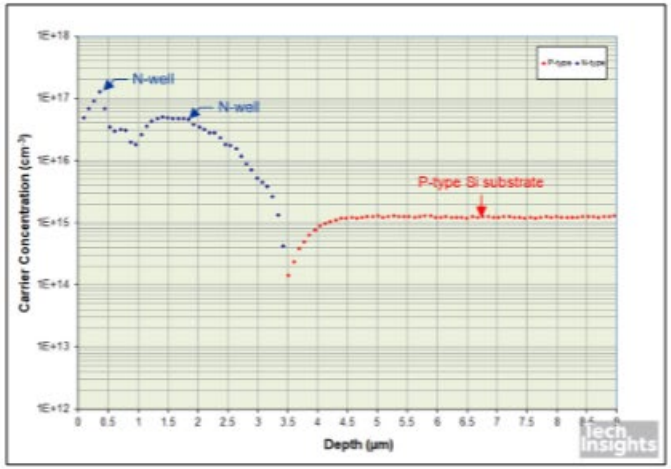
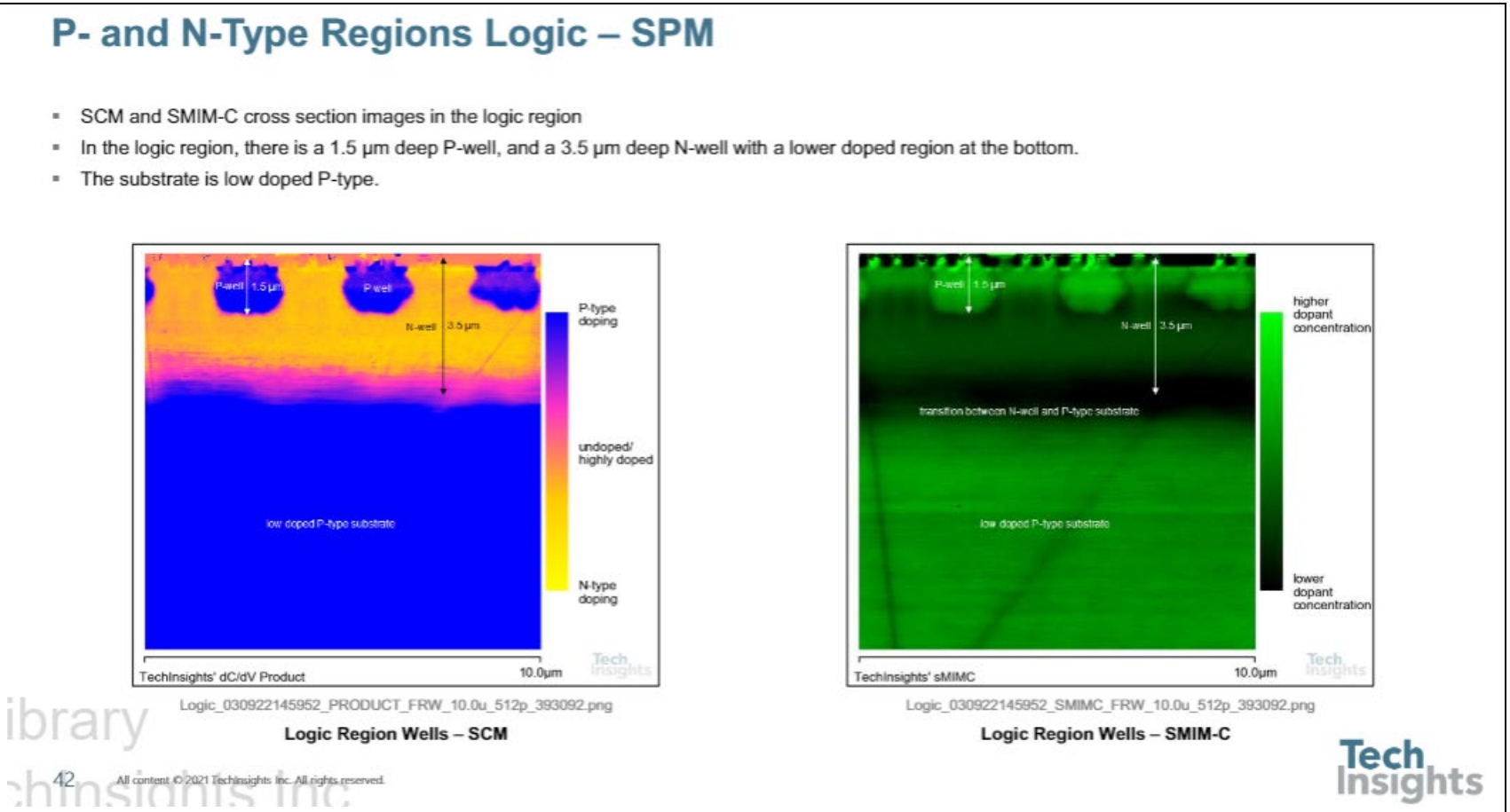
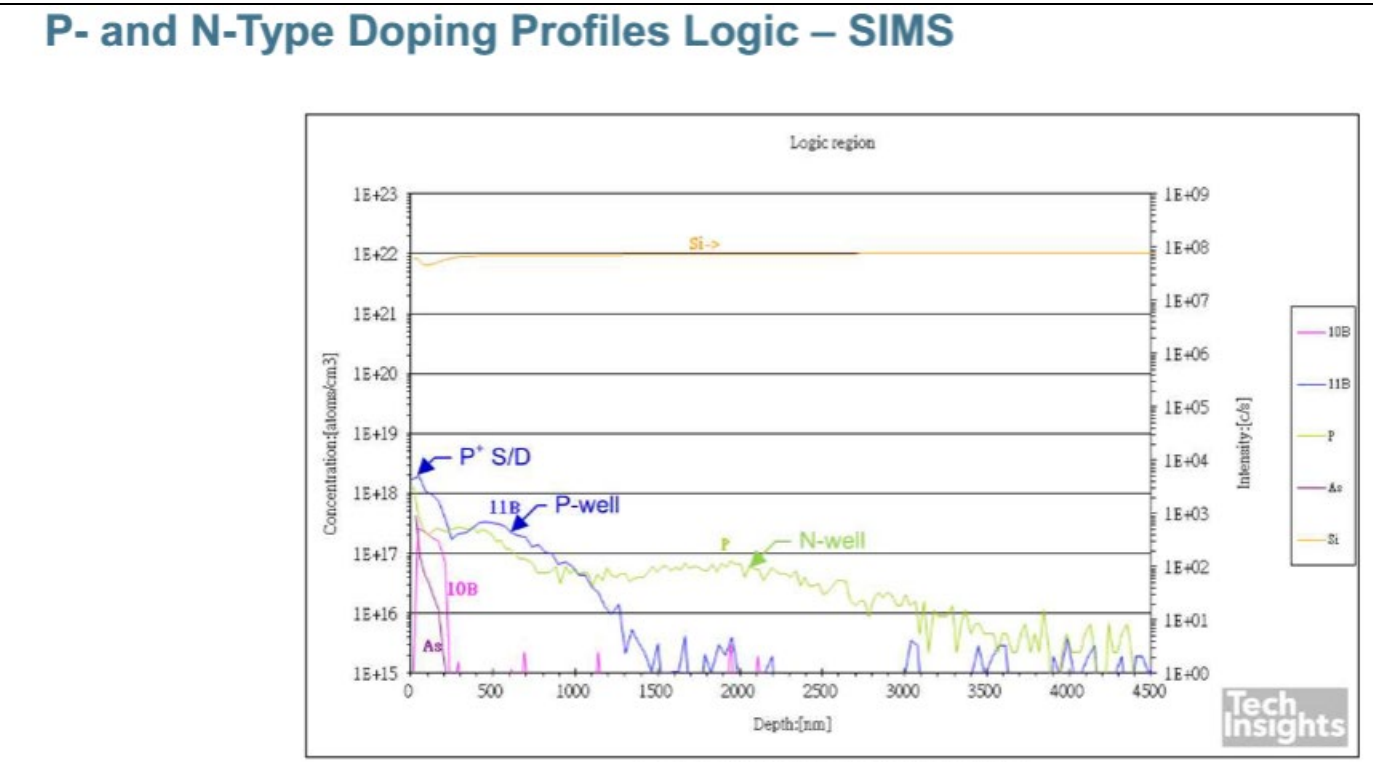
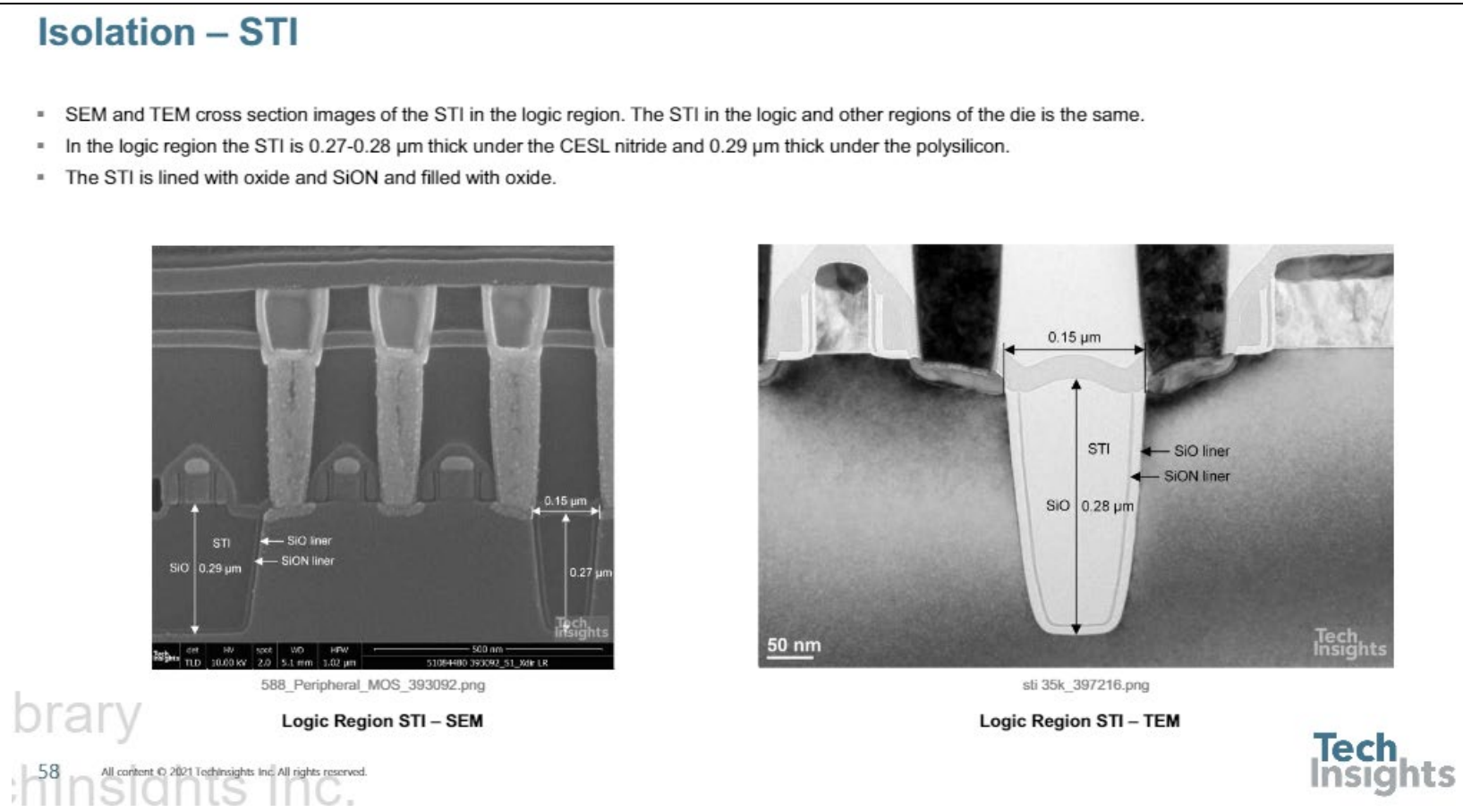
	P- and N-Type Doping Profiles Logic – SRP ▪ SRP doping profile in the logic; probe load 5 Bevel Angle 0.02195 <100> Si X-step 4 µm. ▪ Near the surface, a first N-type doping concentration peak of 1.2×10^{17} cm^{-3}, likely corresponding to the contact region. Then at a depth of about 1.5 µm up to a depth of 3.5 µm, a second N-type doping concentration peak of 5×10^{16} cm^{-3}, which likely corresponds to the N-well. Below a depth of 3.5 µm it is the P-type Si substrate with a doping concentration of about 1.2×10^{15} cm^{-3}.  SRP_Profile_Logic.png **Logic SRP Doping Profile** 55 TMF8828 Report at 55.
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The AMS-OSRAM Accused Products meet this limitation. As shown in the image below, the substrate is a p-type substrate.

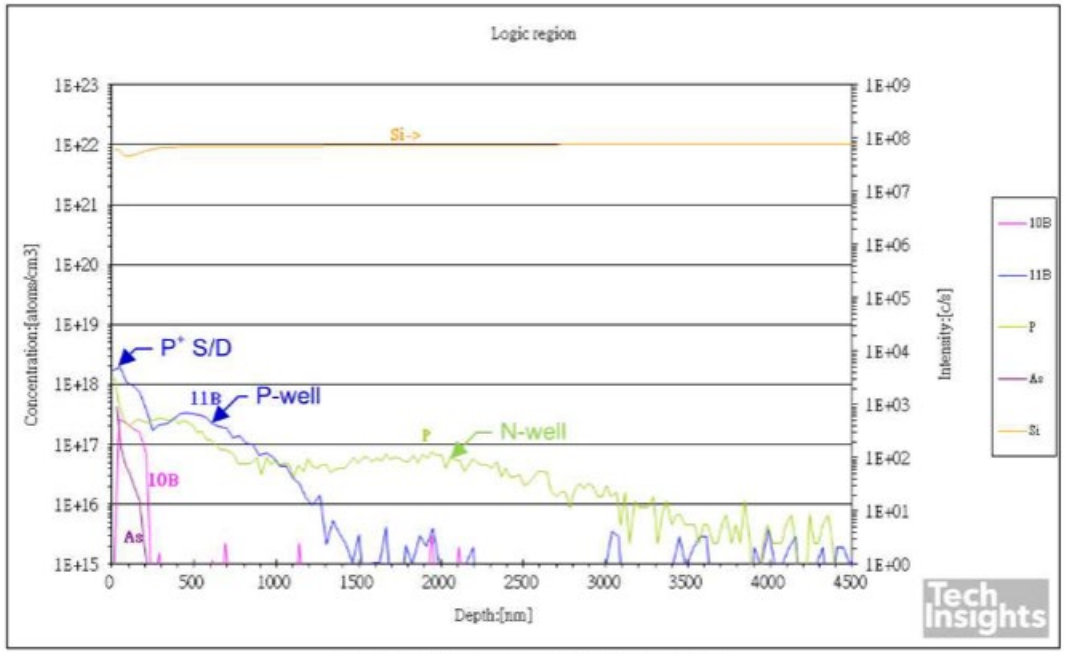
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

	 TMF8828 Report at 42.
3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	Upon information and belief, the substrate of the AMS-OSRAM Accused Products has epitaxial silicon on top of a nonepitaxial substrate. Epitaxial layers are well known in the industry. *See* https://www.powerwaywafer.com/why-do-semiconductor-devices-need-epitaxial-layer.html. Because it is well known in the art, the AMS-OSRAM Accused Products likely meet this limitation.

4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The AMS-OSRAM Accused Products meet this limitation. *See* above, Claim 2.
5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The AMS-OSRAM Accused Products meet this limitation. As shown above, both N-well and P-wells are used in the logic region of this device. The first and second active regions accordingly contain p-channel or n-channel devices. *See* Tech Insights Report images reproduced at Claim 1, Element 2. Each well has a graded dopant, as shown below.

	 SIMS_Analysis_Logic_Region_Doping_Profiles.png **Logic Region Doping Profile – SIMS** 51 TMF8828 Report at 51.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at	Upon information and belief, the substrate of the AMS-OSRAM Accused Products have isolation regions that separate the first and second active regions. As shown below, SEM and TEM cross section images show the use of at least one isolation region (annotated as STI) in the logic region.

least one isolation region.	 TMF8828 Report at 58.
7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the AMS-OSRAM Accused Products. Information about the fabrication process for the AMS-OSRAM Accused Products, including usage of an ion implantation process, is in the possession of Defendants and is expected to be obtained through discovery.
8. The semiconductor	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Elements 1-3.

device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The AMS-OSRAM Accused Products meet this limitation. The SIMS image below indicates graded dopant regions in the first active region or the second active region that are both p-type and n-type. **P- and N-Type Doping Profiles Logic – SIMS**  SIMS_Analysis_Logic_Region_Doping_Profiles.png **Logic Region Doping Profile – SIMS** 51 TMF8828 Report at 51.

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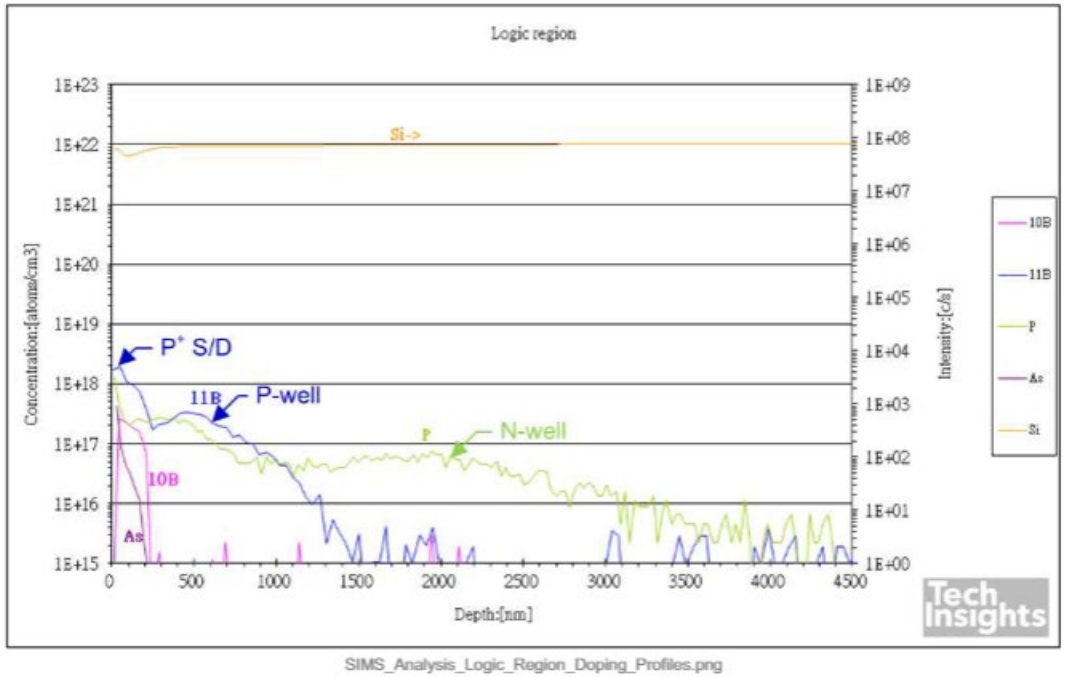
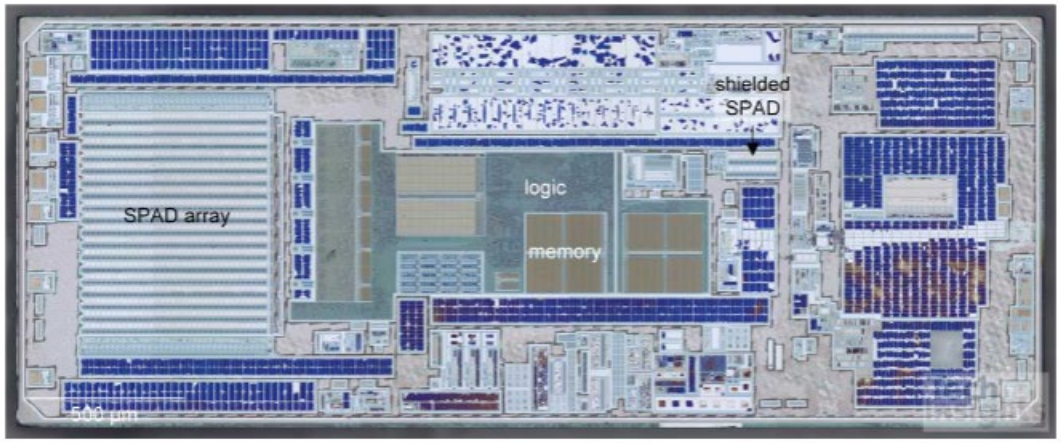
12. The semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.	The AMS-OSRAM Accused Products meet this limitation. The SIMS image below indicates graded dopant regions in well regions that are both p-type and n-type. **P- and N-Type Doping Profiles Logic – SIMS**  SIMS_Analysis_Logic_Region_Doping_Profiles.png **Logic Region Doping Profile – SIMS** 51 All content © 2021 TechInsights Inc. All rights reserved. TMF8828 Report at 51.
13.The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active	The AMS-OSRAM Accused Products meet this limitation. As discussed above for Claim 1, the AMS-OSRAM Accused Products include first and second active regions. Upon information and belief, CMOS transistors are formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendants and are expected to be obtained through discovery.

regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	
15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Claims 3 (regarding nonepitaxial substrate), 13 (regarding CMOS).
17. The semiconductor device of claim 1, wherein the device is a logic device.	The AMS-OSRAM Accused Products meet this limitation. As shown in the block diagram of the figure below, the TMF8828 includes a logic region and is therefore a logic device.

	Annotated d-ToF Die Photograph at Substrate Level  ELZ-AN20_ToF_51084480_391407_Substrate.png TMF8828 Report at 20.
[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include/comprise a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 1, Element 1.

[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 1, Element 4.
[Claim 20, Element 5] at	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 1, Element 5.

least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 6.
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 2.
23. The semiconductor device of claim 20, wherein the substrate has	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 3.

epitaxial silicon on top of a nonepitaxial substrate.	
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 4.
25.The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 5.
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 6.

least one isolation region.	
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 9.
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 7.
32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The AMS-OSRAM Accused Products meet this limitation. *See* Claim 13.
34. The semiconductor device of claim 20, wherein the device is a logic device.	The AMS-OSRAM Accused Products meet this limitation. See above, Claim 17.

Exhibit A-3 to Greenthread's Complaint

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[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a VLSI semiconductor device. AMS-OSRAM TMF8828 ("TMF8828") discussed for claim 1 of Exhibit A-1 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble) with transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery. The AMS-OSRAM TMF8828 is representative of the AMS-OSRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other AMS-OSRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, the other AMS-OSRAM Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Similarly, the other AMS-OSRAM Accused Products would have been designed in a similar manner as the AMS-OSRAM TMF8828 for purposes of this claim chart to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.

Exhibit A-3 to Greenthread's Complaint

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active region or second active region;	
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 5. *See* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. As shown in the SCM/sMIM analysis at Exhibit A-2, Claim 1, Element 6, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the AMS-OSRAM Accused Products are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 2.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 5; Exhibit A-2, Claim 4. As shown in the SCM/sMIM analysis at Exhibit A-2, Claim 1, Element 6, at least some of the transistors form digital logic of the VLSI semiconductor device. *See* above at Claim 1, Element 6.

Exhibit A-3 to Greenthread's Complaint

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logic formed by one of either p-channel and n-channel devices.	
5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 6.
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. *See* above at Claim 1, Element 6.

Exhibit A-3 to Greenthread's Complaint

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regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	
15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-2, Claim 15.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The AMS-OSRAM Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. *See* above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding capacitors in the AMS-OSRAM Accused Products are in the possession of the Defendants and are expected to be obtained through discovery.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The AMS-OSRAM Accused Products meet this limitation. As shown by SEM imaging (*see* Exhibit A-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 9, Element 2.

Exhibit A-3 to Greenthread's Complaint

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[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 9, Element 3.
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 5. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. As shown by SCM/sMIM analysis, SIMS analysis, and SRP analysis (*see* Exhibit A-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SCM/sMIM graph discussed at Exhibit A-1, Claim 1, Element 5. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 2.

Exhibit A-3 to Greenthread's Complaint

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24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 5.
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 6.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-2, Claim 9.
32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 8.

Exhibit A-3 to Greenthread's Complaint

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33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-2, Claim 15.
38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.	The AMS-OSRAM Accused Products meet this limitation. See above at Claim 20.
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a semiconductor device. *See* Exhibit A-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2.
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.

Exhibit A-3 to Greenthread's Complaint

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[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 5; *see* above at Claim 21, Element 5. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 39, Element 3.

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active region and within which transistors can be formed;	
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 5. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 39, Element 3.

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[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The AMS-OSRAM Accused Products meet this limitation. SCM/sMIM analysis, SIMS analysis, and SRP analysis (*see* Exhibit A-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 44, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a CMOS Semiconductor device. *See* Exhibit A-1, Claim 1, Preamble; Exhibit A-1, Claim 18.
[Claim 44, Element 1]: a surface layer;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 21, Element 1.
[Claim 44, Element 2] a substrate;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 44, Element 1.
[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2 (discussion of active region); Exhibit A-1, Claim 18 (discussion of source and drain).

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 21, Element 5. Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants. Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Complaint

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a CMOS semiconductor device. The AMS-OSRAM TMF8828 ("TMF8828") discussed for claim 1 of Exhibit A-3 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble and Exhibit A-3, Claim 44, Preamble) with transistors, and is a CMOS semiconductor device upon information and belief. The AMS-OSRAM TMF8828 is representative of the AMS-OSRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other AMS-OSRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, the other AMS-OSRAM Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). Similarly, the other AMS-OSRAM Accused Products would have been designed in a similar manner as the AMS-OSRAM TMF8828 for purposes of this claim chart to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a surface layer;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 1.
[Claim 1, Element 2] a substrate;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 2.
[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 3.
[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer (*see* Exhibit A-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally are discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Complaint

U.S. Patent No. 8,421,195	Accused Products
carriers from said surface layer to said substrate; and	
[Claim 1, Element 5] at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally are discussed at Exhibit A-1, Claim 1, Element 5.
2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.	The AMS-OSRAM Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer.
3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 4; Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer.
5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1, 5.
6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1, 5.

Exhibit A-5 to Greenthread's Complaint

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Preamble] A semiconductor device comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include a semiconductor device. The AMS-OSRAM TMF8828 ("TMF8828") discussed for claim 1 of Exhibit A-1 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble) with transistors, and is a semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery. The AMS-OSRAM TMF8828 is representative of the AMS-OSRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other AMS-OSRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, the other AMS-OSRAM Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). Similarly, the other AMS-OSRAM Accused Products would have been designed in a similar manner as the AMS-OSRAM TMF8828 for purposes of this claim chart to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 7, Element 1] a surface layer;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 1.
[Claim 7, Element 2] a substrate;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 2.
[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 3.
[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 4. The graded concentration of dopants observed via SCM/sMIM analysis, SIMS analysis, and SRP analysis (*see* Exhibit A-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally are discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-5 to Greenthread's Complaint

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 5. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally are discussed at Exhibit A-1, Claim 1, Element 5.
8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.	The AMS-OSRAM Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally are discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include an electronic system. *See* Exhibit A-1, Claim 1, Preamble; Exhibit A-4, Claim 1, Preamble. Each AMS-OSRAM Accused Product is an electronic system, because the sensor has electronic components such as transistors. The AMS-OSRAM TMF8828 is representative of the AMS-OSRAM Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other AMS-OSRAM Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, the other AMS-OSRAM Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Similarly, the other AMS-OSRAM Accused Products would have been designed in a similar manner as the AMS-OSRAM TMF8828 for purposes of this claim chart to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other AMS-OSRAM Accused Products contain similar features as the AMS-OSRAM TMF8828, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 2; Exhibit A-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 3; Exhibit A-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 4.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 5. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally are discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 6; Exhibit A-3, Claim 21, Element *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally are discussed at Exhibit A-1, Claim 1, Element 5.6.
2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 2.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 4.
5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 5.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 8.
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 15.
16. The system of Claim 1, wherein the at least one semiconductor device is a flash memory.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 16.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 17.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 20.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the AMS-OSRAM Accused Products include an electronic system. *See* above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1c; Exhibit A-1, Claim 9, Element 2.
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1d; Exhibit A-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1e.
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1f; Exhibit A-1, Claim 9, Element 5. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally are discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
area of the substrate where there are no active regions; and	
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The AMS-OSRAM Accused Products meet this limitation. *See* above at Claim 1, Element 1g; Exhibit A-3, Claim 21, Element 6. *See also* SCM/sMIM analysis, SIMS analysis, and SRP analysis reproduced at Exhibit A-1, Claim 1, Element 5, electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis, SIMS analysis, and SRP analysis generally are discussed at Exhibit A-1, Claim 1, Element 5.
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 26.
27. The system of Claim 21, wherein the first active region and second active region of the at least	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 27.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
one semiconductor device are each separated by at least one isolation region.	
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The AMS-OSRAM Accused Products meet this limitation. *See* Exhibit A-3, Claim 28.

Tech Insights

techinsights.com

ams OSRAM
TMF8828, 17 µm × 39 µm Pixel Pitch d-ToF Sensor from Honor Magic3 Pro Rear-Facing Camera

Device Essentials Plus Summary

DEP-2110-801

111404OOWM

Published: April 8, 2022

DEP Content

- This is a Device Essentials Plus (DEP) summary document, provided as a companion deliverable for a Device Essentials Plus project. The DEP deliverable builds on the content generated in a Device Essentials (DEF) project
- The DEF deliverable includes an analysis summary document and a pixel schematic, and is supported by unannotated image folders including:
  - Package photographs and X-rays, die photograph, non-invasive optical photos of die features, scanning electron microscopy (SEM) bevel images of the pixel array showing the metal, transistor, and diffusion levels, exploratory cross-sectional SEM images of the general pixel array and peripheral structures
- The purpose of the DEP is to extend coverage of chip analysis beyond the SEM-based imaging used for DEF projects, and to expand the analyst commentary. A DEP contains interpreted results from transmission electron microscopy (TEM), TEM-based energy dispersive X-ray spectroscopy (TEM-EDS), secondary ion mass spectroscopy (SIMS) and scanning capacitance microscopy (SCM) analyses (the DEP scope is target device dependent).
- This DEP report includes a summary of salient features of the device and is supported with the following image folders:
  - TEM images of pre-metal dielectrics (PMD) and microlens
  - TEM-EDS spectra of dielectrics, metals, and microlens
  - Scanning microwave impedance microscopy (SMIM) of the pixel photocathode along horizontal and vertical planes of cross-section, and periphery
  - SIMS analysis of the CMOS image sensor (d-TOF) die pixel array
  - SRP analysis of the d-TOF die pixel array and periphery

Overview

- The ams OSRAM TMF8828 is a configurable 8x8 multi-zone direct time-of-flight (d-ToF) sensor [1] [2] extracted from the Huawei Honor Magic3 Pro (ELZ-AN10).
- The TMF8828 comes in a 12-pin organic land grid array (OLGA) package, which houses a single photon avalanche diode (SPAD) die, a 940 nm vertical cavity surface emitting laser (VCSEL) and physical infrared filters [1].
- The TMF8828 can measure a distance ranging from 10 mm up to 5 m [1].
- The TMF8828 SPAD die is a front-illuminated (FI) d-ToF with a multi-layer filter over the active and shielded SPAD arrays, and other circuits of the die, and uses a SPAD sensor for detection [1].
- The active SPAD array is organized as 34 × 18 SPADs, with a pixel pitch of 17 µm × 39 µm.

Device Summary

Device Summary

Manufacturer	ams OSRAM
Foundry	Likely ams OSRAM
Part number	TMF8828
Type	FI d-ToF
Die thickness	150 µm
Die size, measured from the die edge	3.26 mm × 1.31 mm (4.3 mm^2)
Process type	FI CMOS ToF
Number of metal layers	6 Cu, 1 Al, 1 Al MIM capacitor bottom electrode and 1 Ta-based top electrode
Number of poly layers	1
Contacted logic gate pitch	240 nm (SRAM CGP 220 nm)
Minimum metal pitch logic	180 nm
Minimum metal pitch pixel array	170 nm
Process generation	65 nm
Features measured to determine process generation	Logic contacted gate pitch, and minimum metal pitch

Salient Features

General Package

- LGA package
  - Package measures 4.6 mm × 2.0 mm × 1.5 mm thick
  - 12 lands with a 0.82 mm pitch
  - Single row of bond pads, with a minimum pitch of 81 µm, arranged along the left and right sides of the die, are used to connect the die to the organic printed wiring board (PWB).
  - Gold (Au) solder pad formed over the bond pads and Au bonding wires
  - VCSEL die attached to a solder pad region on the top surface of the SPAD die
  - Package opening over the VCSEL with an infrared (IR) filter
  - Package opening over the active SPAD array with a lens
  - Optical isolation wall between active SPAD array and VCSEL

Salient Features

General Logic Region

- The d-TOF die was likely manufactured by ams OSRAM in a 65 nm CMOS process [4].
- 140 µm thick substrate, comprising a bulk P-type silicon (Si) substrate
- The minimum logic gate length is 57 nm
  - Contacted gate pitch (CGP) of 240 nm
  - 95 nm thick silicided polysilicon gate
  - Polysilicon gate and source/drain (S/D) regions use nickel platinum (NiPt) silicide
  - The gate dielectric comprises a 2.8 nm nitrided oxide
- Tungsten (W) contact with titanium nitride (TiN) liner
- Six copper (Cu) interconnect layers
  - Minimum metal pitch of 180 nm
  - Metal 1 is single Cu damascene with a tantalum (Ta) based liner, and metal 2 through metal 6 are dual Cu damascene also with Ta-based liners.
  - Metal 6 is 0.85 µm thick dual copper damascene with a 20 nm thick Ta-based liner. Metal 7 Al is not used in the logic region
- The same pre-metal dielectrics (PMD) and interlayer dielectrics (ILD) layers were observed in the logic, SPAD readout circuitry and SPAD regions.
  - The PMD comprises a SiON liner and pad oxide, a CESL nitride, a PMD 1 SiOP, a PMD 2 SiOC, a PMD 3 oxide, and a PMD 4 SiOC.
  - ILD 1 to ILD 4 comprise a SiCN metal seal layer, a thin oxide, and SiOC metal trench layer
  - ILD 5, which is partial etched over the SPAD region, comprises a 44 nm thick ILD 5-1 nitride, a 0.57 µm thick ILD 5-2 oxide, a 53 nm thick ILD 5-3 nitride, and a 0.76 µm thick ILD 5-4 oxide.
  - The top layers of IMD 6 (IMD 6-3 and IMD 6-4) were etched in the logic region and most of the periphery during the metal 7 Al etch. In the logic region, IMD 6 comprises a 75 nm thick IMD 6-1 nitride and a thinned 0.13 µm thick IMD 6-2 oxide.
  - The passivation comprises a 0.27 µm thick passivation 1 oxide and a 95 nm thick passivation 2 oxide.

Salient Features

General Periphery Region

- MIM capacitors formed in ILD 5, between metal 5 and metal 6.
  - Bottom electrode: 20 nm thick bottom metal barrier, a 160 nm thick Al body, and a 62 nm thick Ta-based top metal barrier.
  - Dielectric: 31 nm thick nitride
  - Top electrode: 73 nm thick Ta-based layer
  - Capping layer: 24 nm thick oxide, and a 46 nm thick nitride
- IMD 6 is partially etched in the logic and SPAD region. The full thickness is only observed under the VCSEL solder pad and in the bond pad regions. IMD 6 comprises a 74 nm thick IMD 6-1 nitride, a 0.20 µm thick IMD 6-2 oxide, a 52 nm thick IMD 6-3 nitride, a 59 nm thick IMD 6-4 oxide.
- Metal 7 is only used under the VCSEL solder pad and in the bond pad regions. Meta 7 comprises a 0.14 µm thick TaN barrier, a 0.96 µm thick Al body, and 32 nm thick Ti-based barrier.
- The VCSEL solder pad comprises a 0.32 µm thick Au liner and 9 µm thick Au body.

Salient Features

General SPAD Readout Circuitry Region

- The minimum logic gate length is 57 nm, same as in the logic region
  - Contacted gate pitch (CGP) of 230 nm
  - 94 nm thick silicided polysilicon gate
  - Polysilicon gate and source/drain (S/D) regions use nickel platinum (NiPt) silicide
  - The minimum pitch transistor gate dielectric comprises a 2.8 nm nitrided oxide
  - Wider and longer transistors are also used in the SPAD readout circuit. The longer transistor gate dielectric is 3.7 nm thick nitrided oxide.
- Same dielectric layers as in the SPAD region
- Six Cu interconnect layers

Salient Features

SPAD Array

- The SPAD array uses five Cu interconnect layers
  - Minimum metal pitch of 170 nm
  - Metal 1 is single Cu damascene with Ta-based liner, and metal 2 through metal 5 are dual Cu damascene also with Ta-based liners.
  - Metal 6 Cu and metal 7 Al are not used in the SPAD region
- The same pre-metal dielectrics (PMD) and interlayer dielectrics (ILD) layers were observed in the logic, SPAD readout circuitry and SPAD regions.
  - The PMD comprises a SiON liner and pad oxide, a CESL nitride, a PMD 1 SiOP, a PMD 2 SiOC, a PMD 3 oxide, and a PMD 4 SiOC.
  - ILD 1 to ILD 4 comprise a SiCN metal seal layer, a thin oxide, and SiOC metal trench layer
  - ILD 5, which is partially etched over the SPAD region, comprises nitride and oxide layers.
- Stand alone (non-shared) pixel architecture, with 17 µm × 39 µm SPAD horizontal and vertical pitches.
- Active SPAD array
  - Organized in 18 rows by 34 columns, yielding an array of 612 total active sensing SPAD pixels.
  - The SPAD rows are interleaved with rows of SPAD readout circuitry.
  - The active SPAD has a metal 5 aperture grid with a fill factor (FF) of 53.3%.
  - The anode is 0.72 µm deep P-type. At the center of the anode is the contact with a 0.25 µm deep P^+ region, with a lower doped P-type region between the P^+ region and the N-type cathode. An approximate 54 nm deep surface region of the anode is higher doped than the anode body. At the top edge, surrounding the anode there is a lower doped P-type guard ring.
  - The cathode is about 4.5 µm deep and has an ~3.6 µm deep higher doped upper region and an ~0.90 µm deep lesser doped lower region. The cathode contact is 0.25 µm deep N^+ region, with a lower doped N-type region surrounding it.

Salient Features

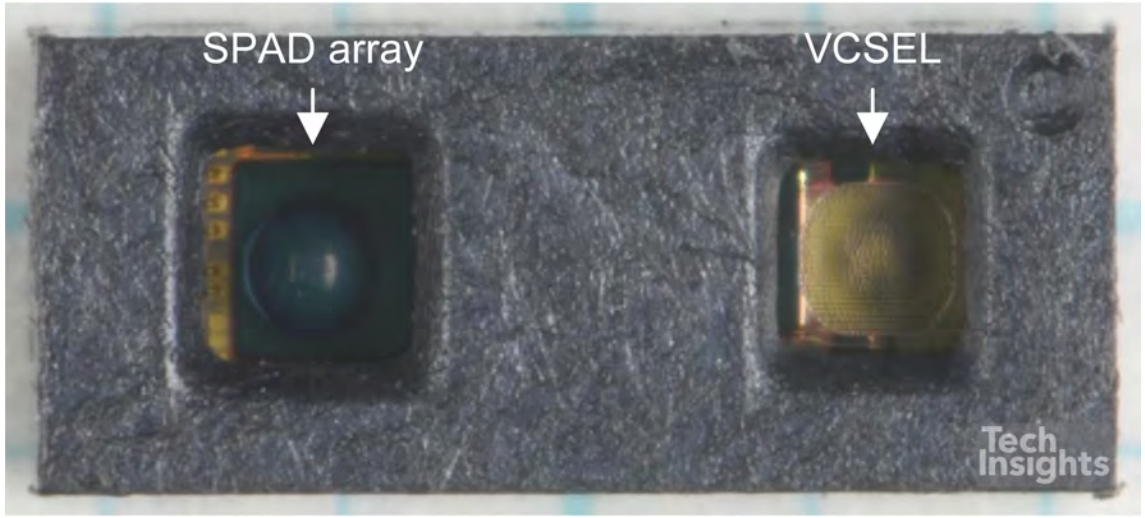
Shielded SPAD Array

- Dark SPAD array
  - The shieled SPAD array is organized in two rows by nine columns, yielding an array of 18 total dark SPAD pixels.
  - The shielded SPAD pitch is the same as the active SPAD
  - The shieled SPAD top metal has an opening of 12.5 µm × 12.5 µm.
  - Lower metal layers have progressively smaller openings, with the smallest one having an opening of about 1.2 µm square.

Package and Die

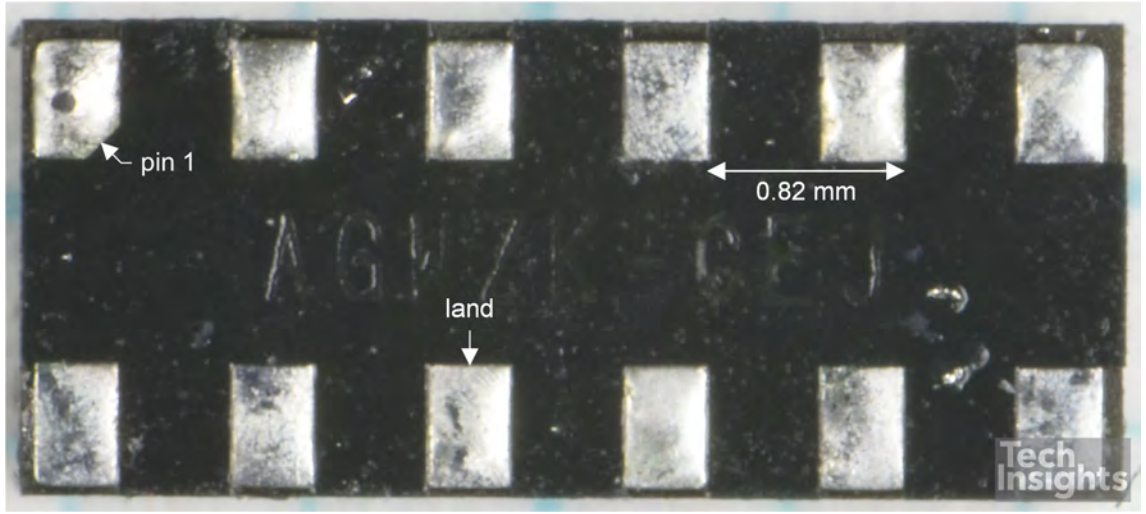
Package Photograph – TMF8828

- 12-pin LGA package containing SPAD chip and a VCSEL light source mounted on the SPAD die
- Package dimensions: 4.6 mm × 2.0 mm × 1.5 mm thick, with a land pitch of 0.82 mm
- Molding compound used as a barrier between the active sensing SPAD array and the dark reference SPAD array
- Square package window over the VCSEL light source with a filter attached to the bottom side of the window.
- The package window over the SPAD receiver array has a square opening with a microlens.
- For more details about the package, refer to TechInsights package report PKG-2110-801 [3].



ELZ-AN10_ToF_Pkg_Top_390683.png

Top

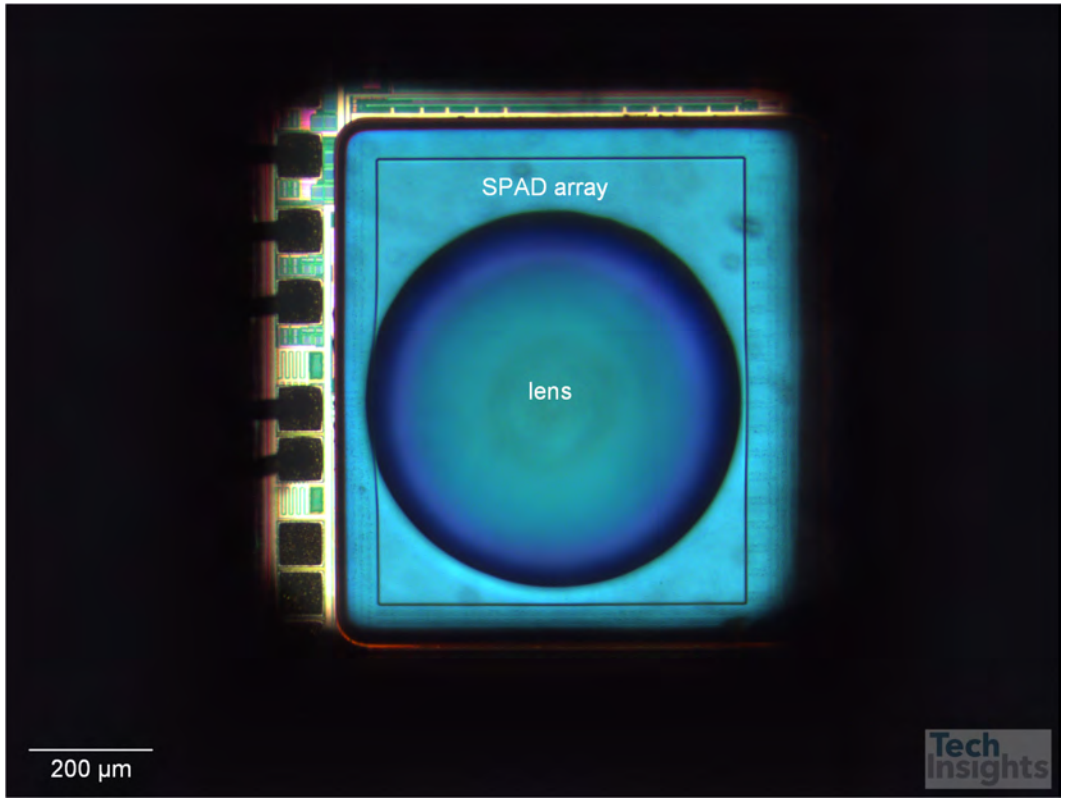


ELZ-AN10_ToF_Pkg_Bot_390683.png

Bottom

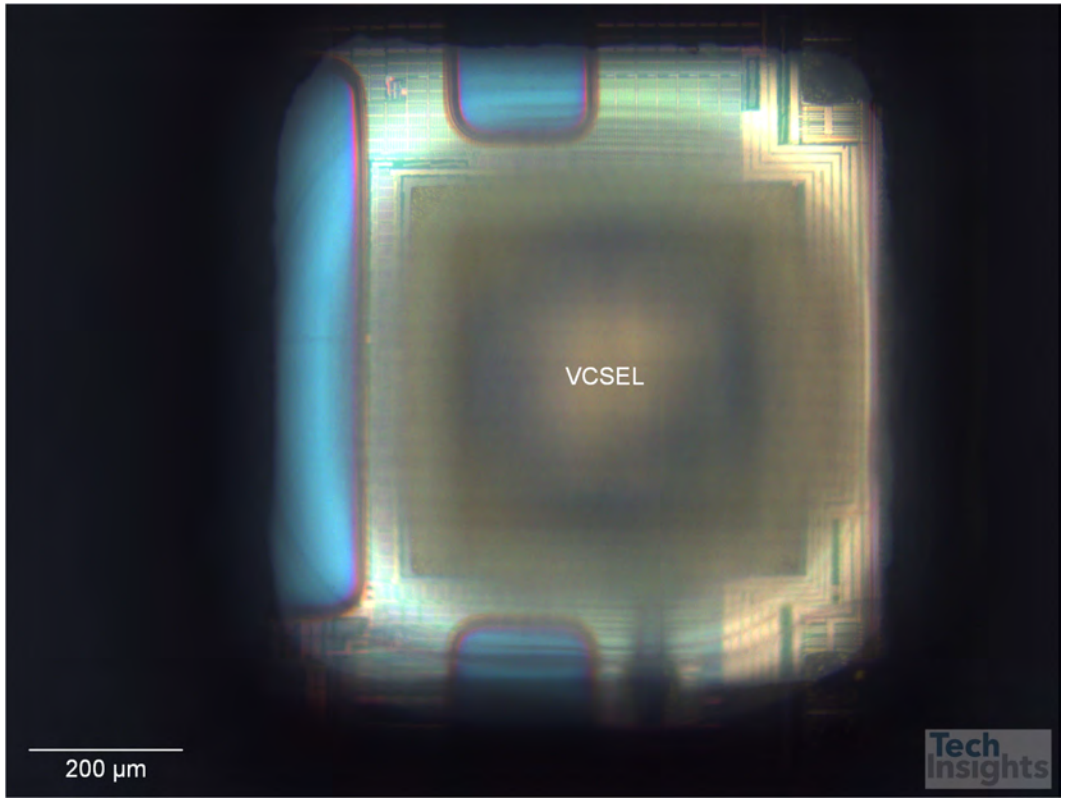
Package Photograph – TMF8828

- Optical images showing the window opening over the active SPAD array (left) and VCSEL (right)



ELZ-AN10_ToF_Pkg_Top_Left_390683_5x1p6r.png

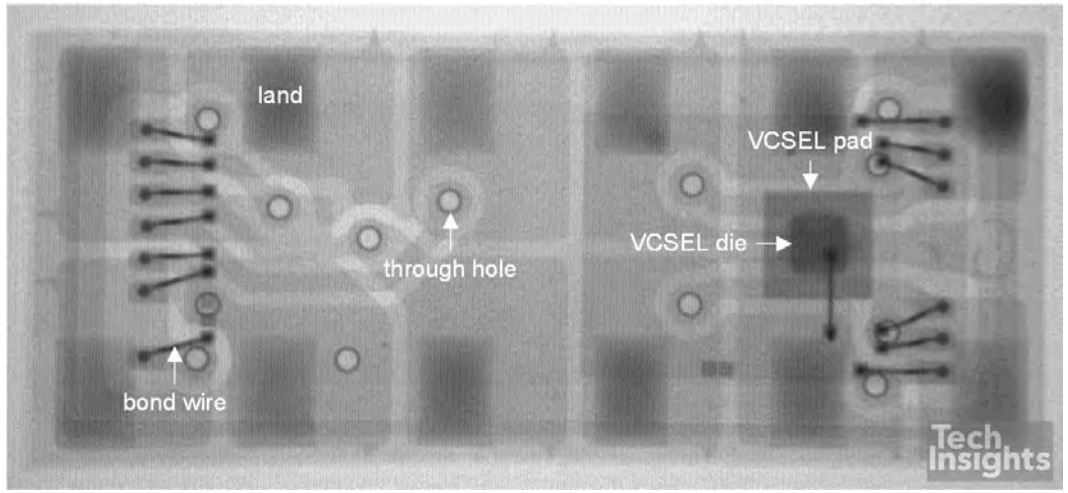
Window Opening Over the SPAD Array – Optical



ELZ-AN10_ToF_Pkg_Top_Right_390683_10x1r.png

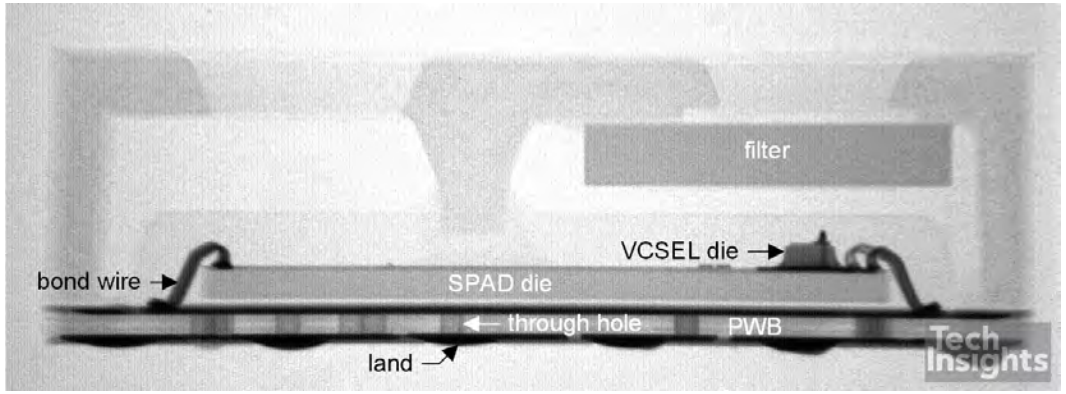
Window Opening Over the VCSEL – Optical

Package X-Rays



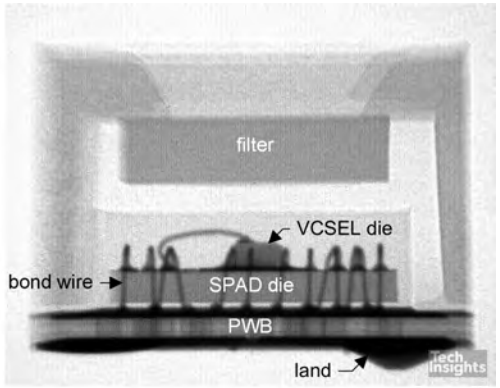
ELZ-AN10_ToF_Xray_Top_390683.png

Top



ELZ-AN10_ToF_Xray_SideA_390683.png

Side A

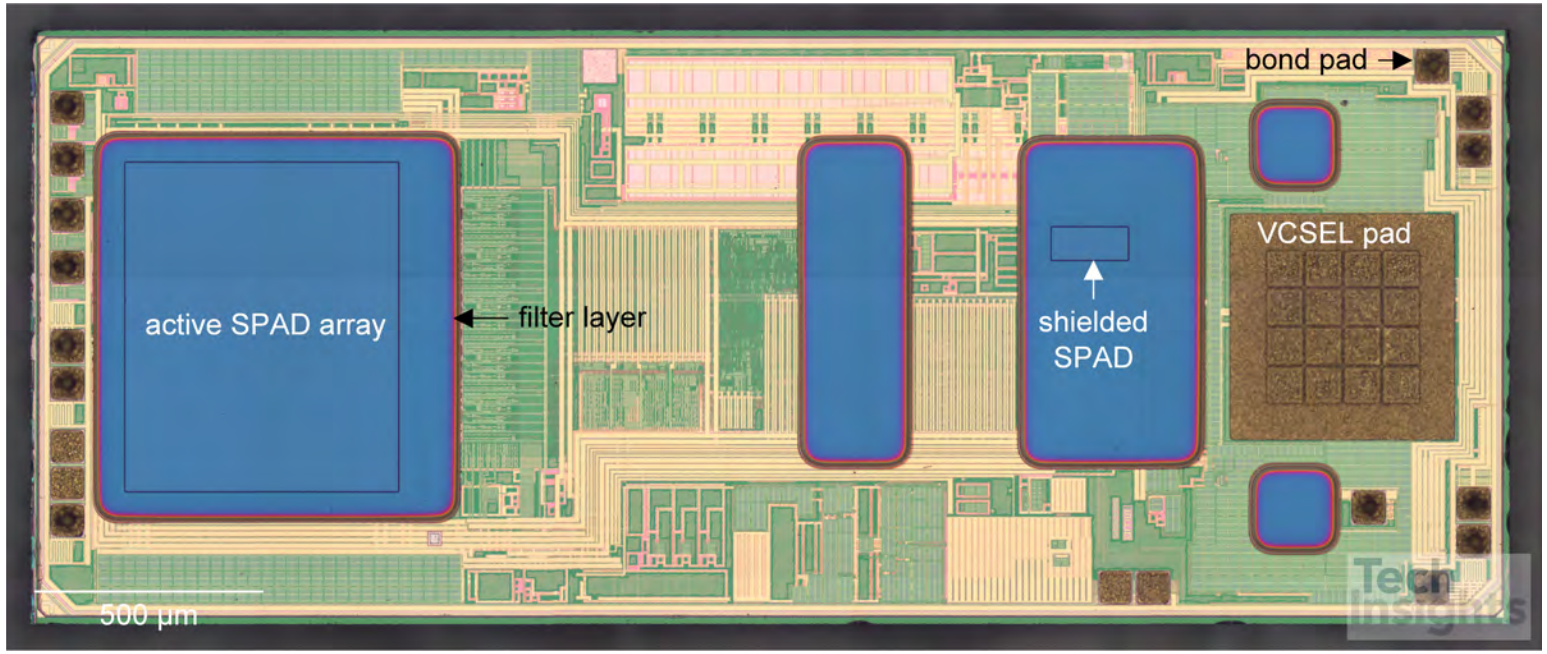


ELZ-AN10_ToF_Xray_SideB_390683.png

Side B

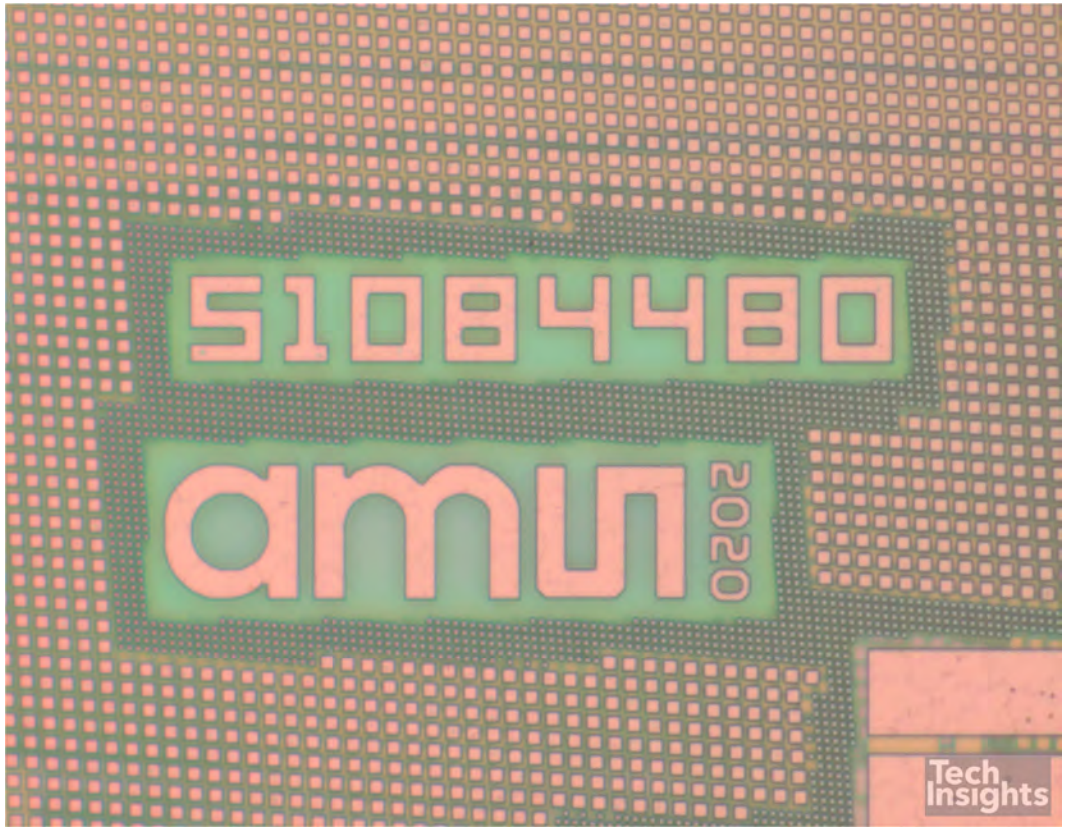
Annotated d-ToF Die Photograph

- The TMF8828 die measures 3.26 mm × 1.31 mm (4.3 mm^2) from the die edge, and 3.23 mm × 1.28 mm (4.1 mm^2) from the die seal.



ELZ-AN10_ToF_51084480_390722_Oriented.png

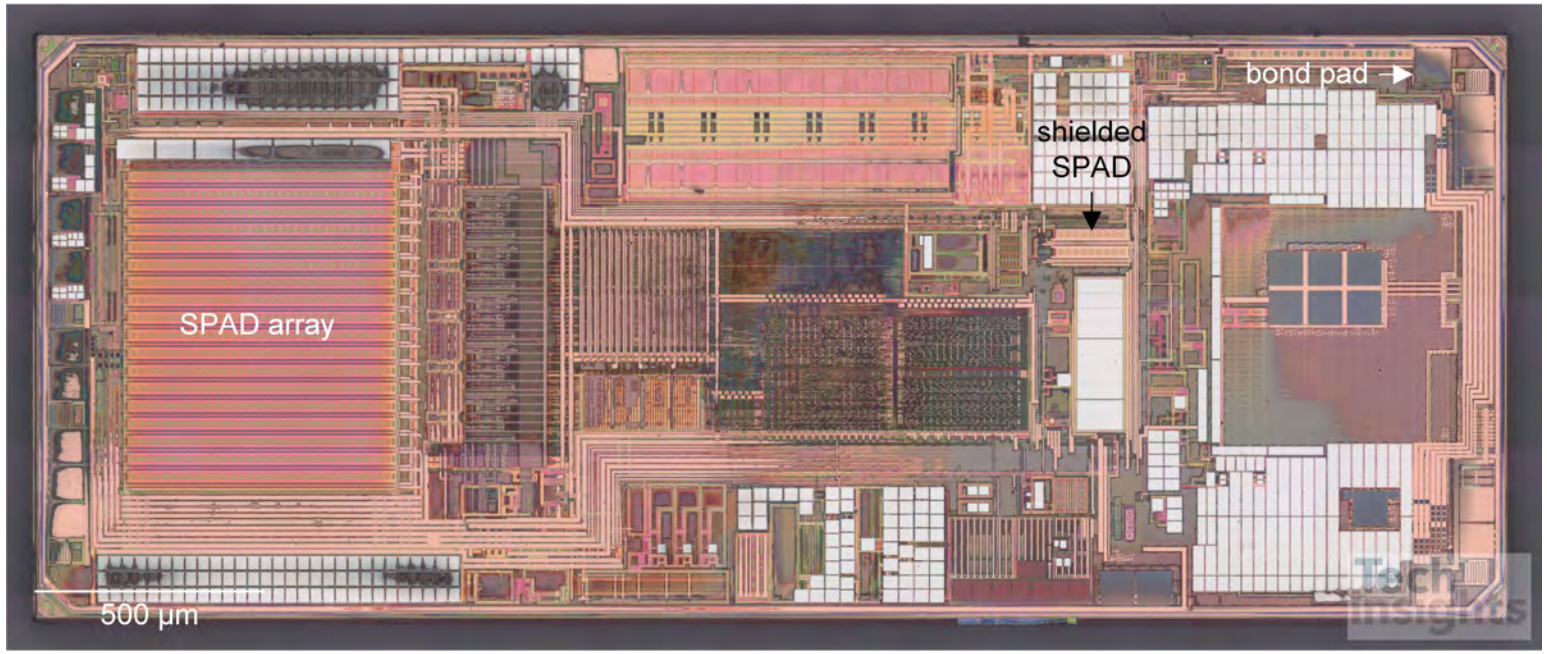
Die Markings



ELZ-AN10_ToF_51084480_390722_DieMrkRotated.png

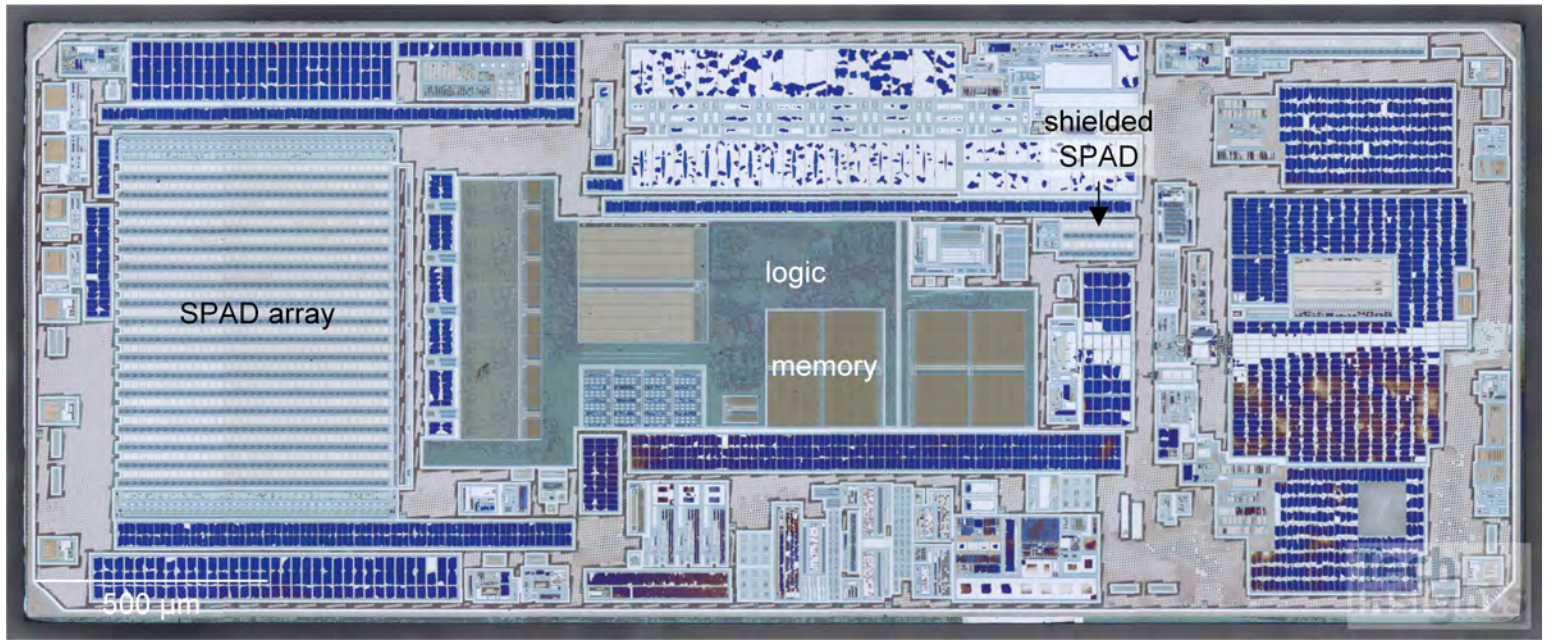
Annotated d-ToF Die Photograph at Metal 6 Level

- The active SPAD array is organized as 34 × 18 SPADs (total 612).
- The shielded SPAD array is organized as 2 × 9 SPADs (total 18).



ELZ-AN20_ToF_51084480_391407_M6.png

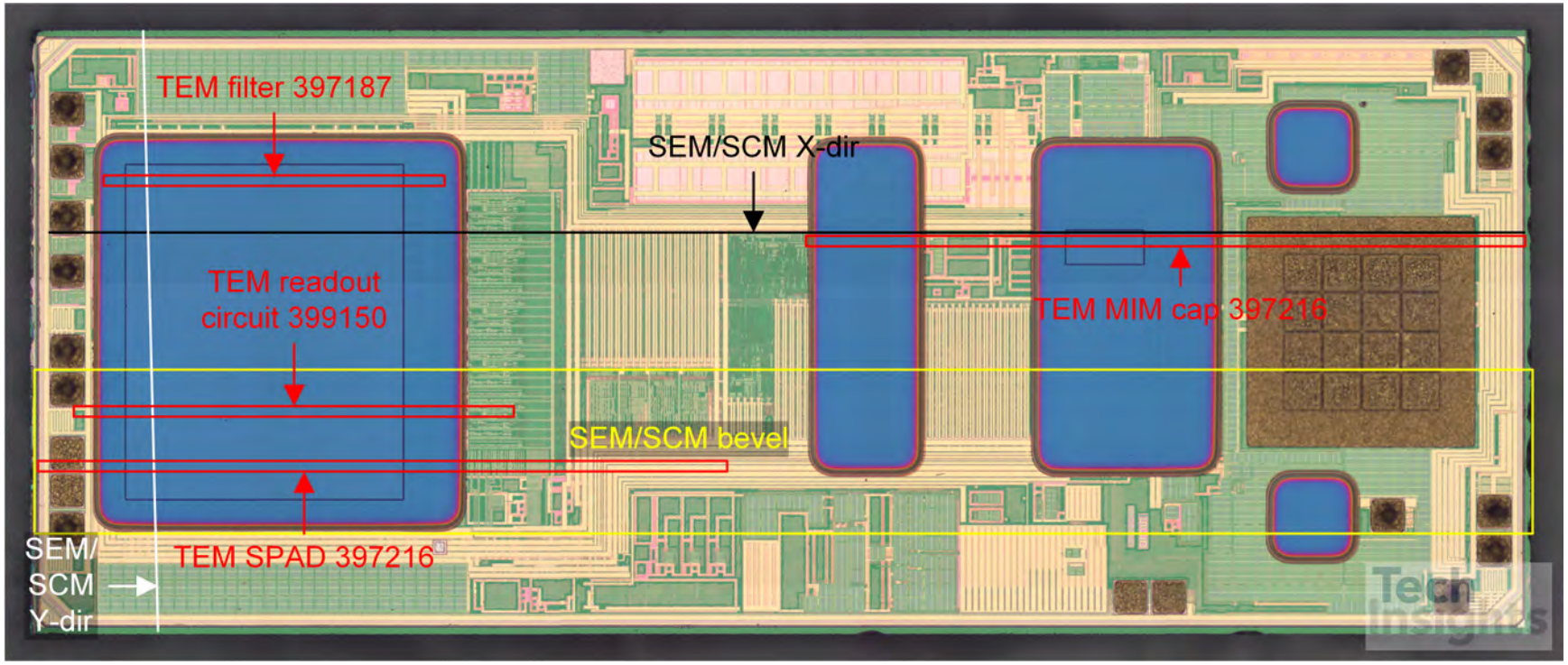
Annotated d-ToF Die Photograph at Substrate Level



ELZ-AN20_ToF_51084480_391407_Substrate.png

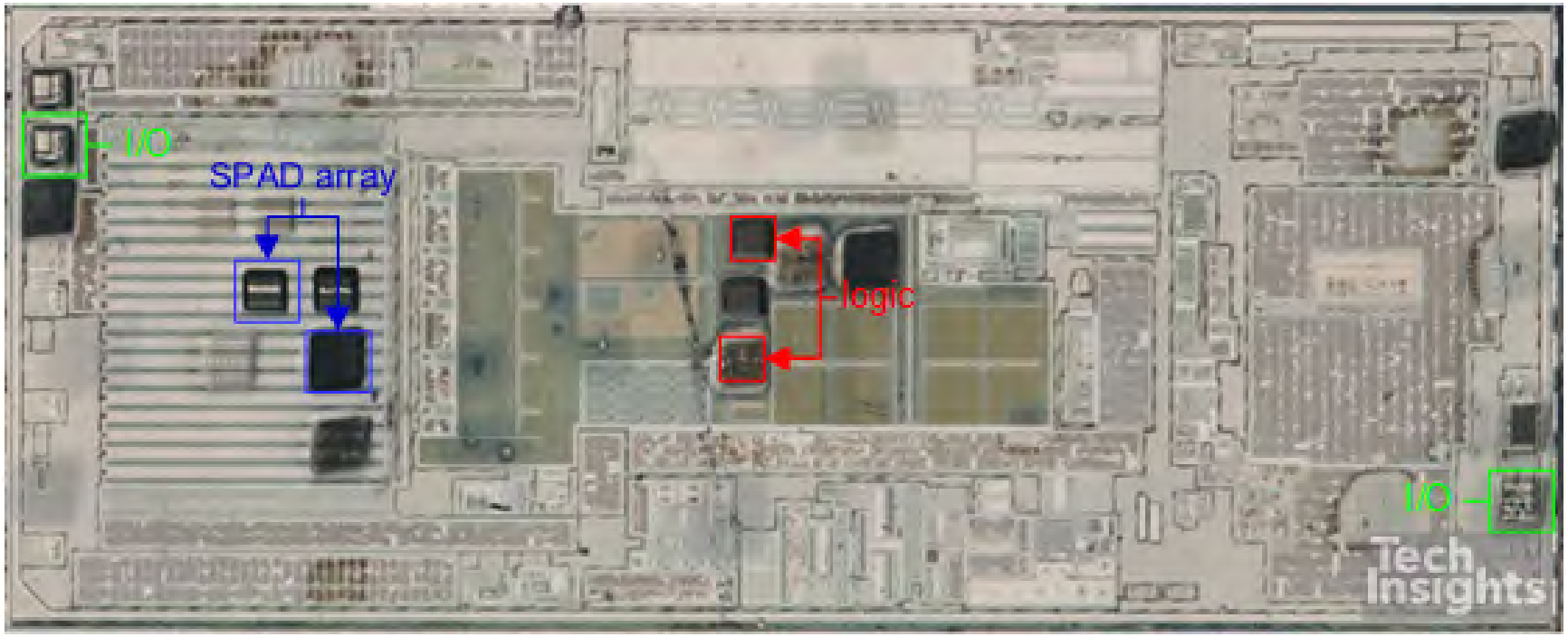
Sample Locations

Analysis Locations – SEM, SCM, and TEM



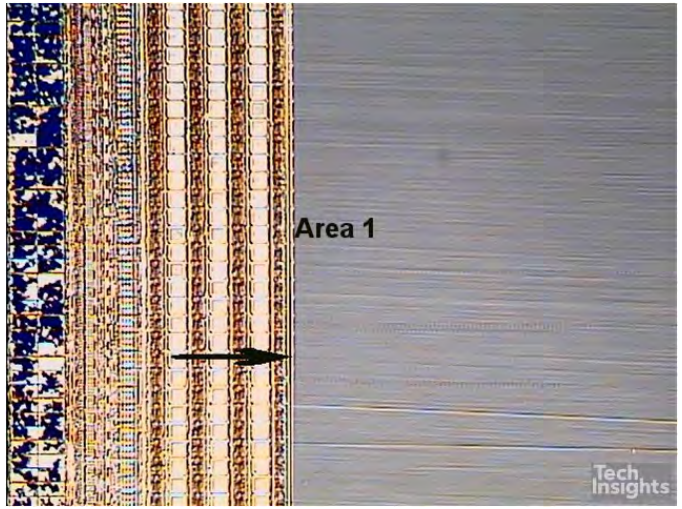
TMF8828_Analysis_Locations.png

Analysis Location – SIMS



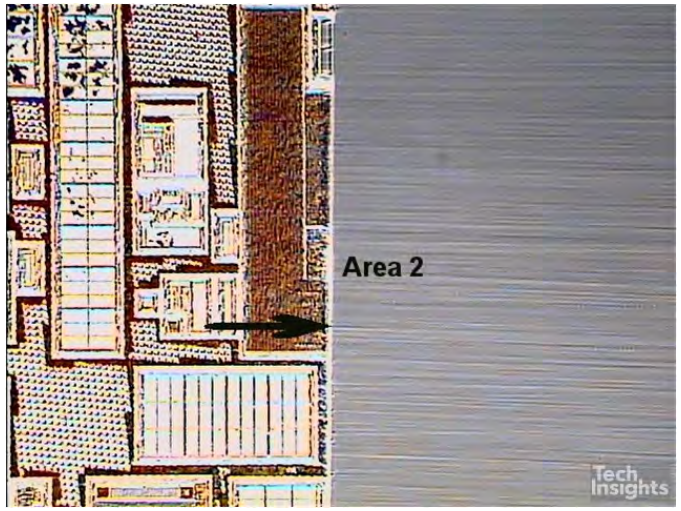
SIMS_Sample.png

Analysis Location – SRP



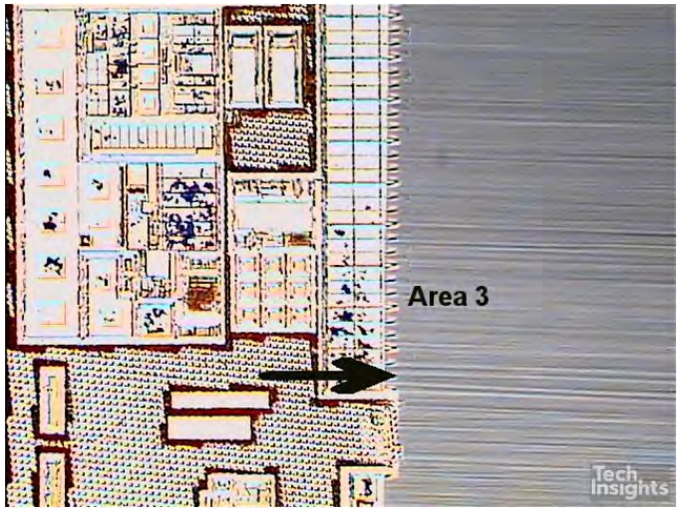
Area_1_SPAD_20Xc1.png

SPAD Array



Area_2_Logic_20XC1.png

Logic



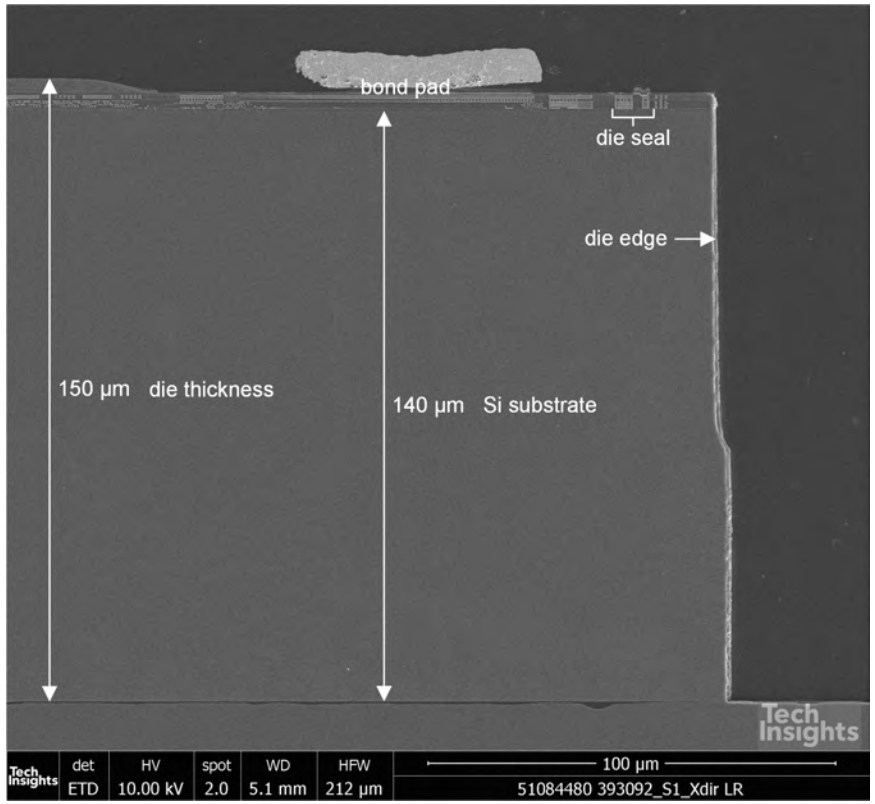
Area_3_Periphery_20XC1.png

Periphery

General Structure

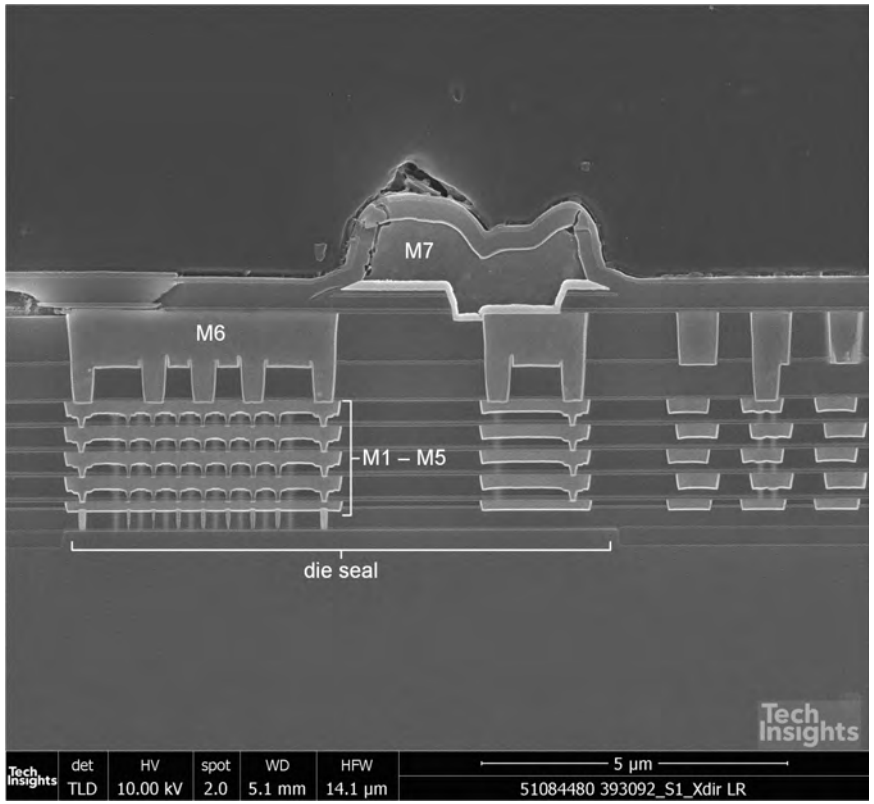
General Structure – Periphery

- Si substrate thickness is 140 µm, and the total die thickness is 150 µm
- The die uses six Cu interconnect layers and one top Al layer



500_Die_Edge_393092.png

Die Thickness

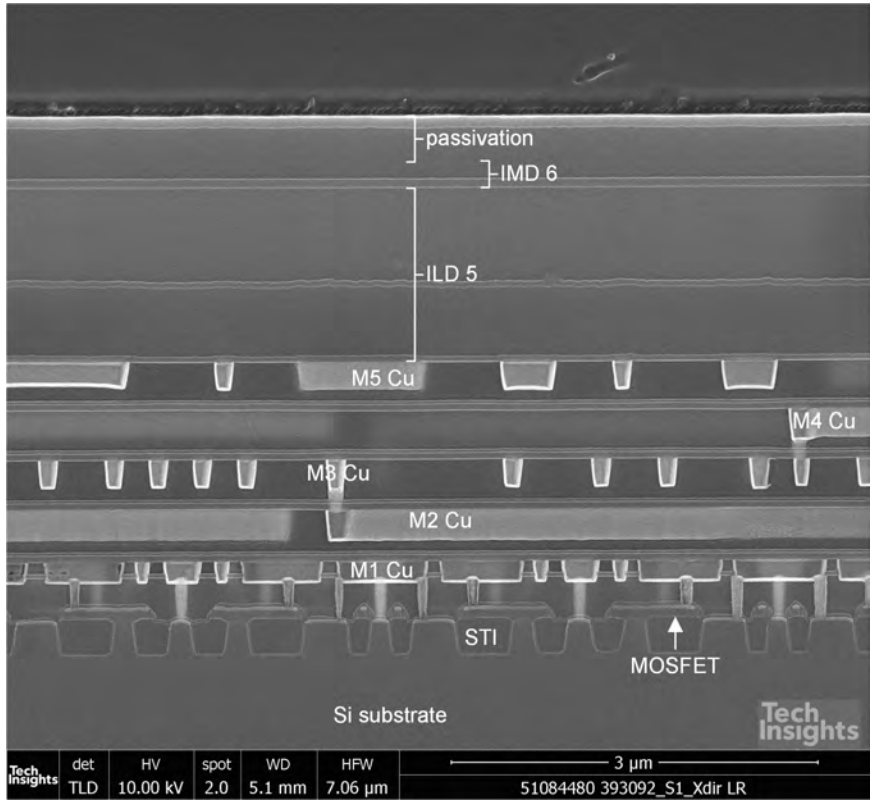


503_Die_Seal_393092.png

Die Seal

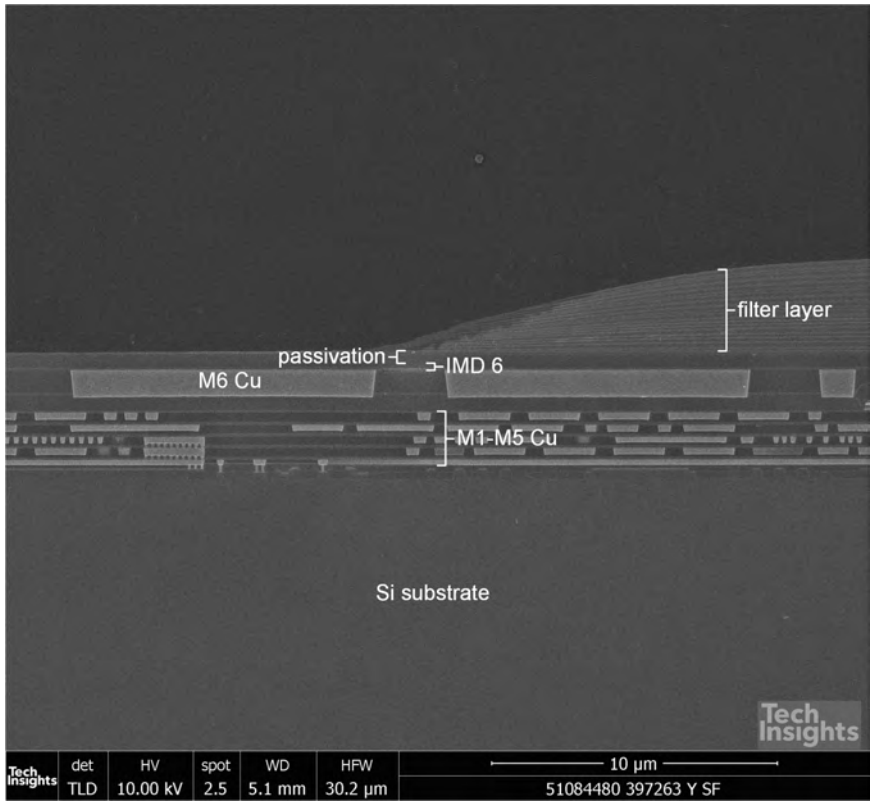
General Structure – Periphery

- The periphery used six Cu interconnect layers and a passivation layer over IMD 6.
- The SPAD array and some other regions of the die are covered with a filter layer.



558_General_Structure_393092.png

General Structure – Periphery

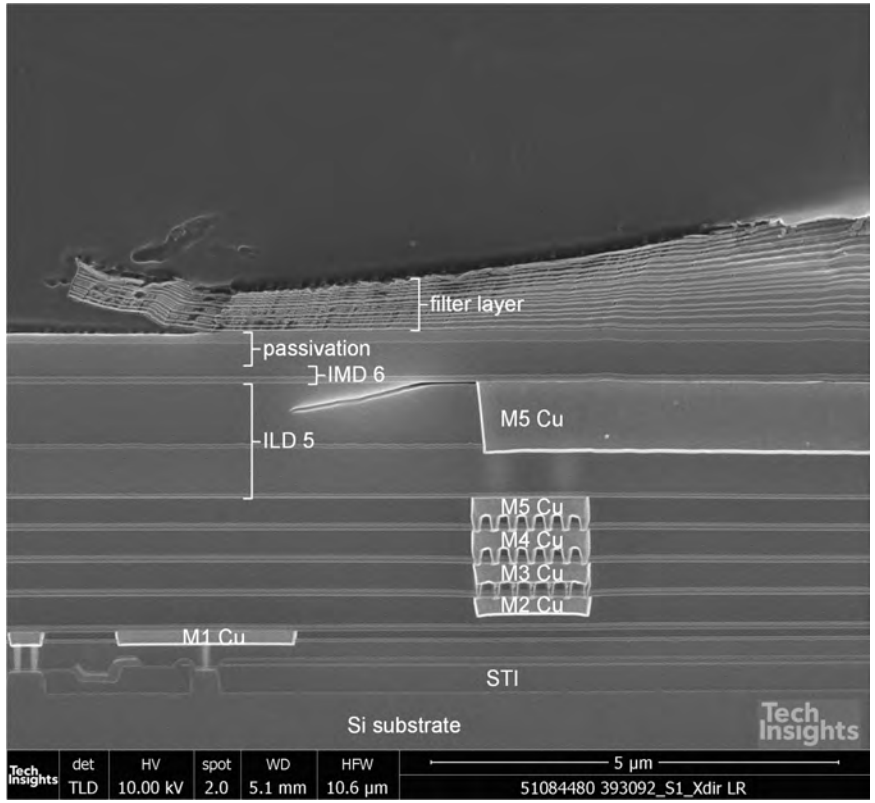


012_periphery_filter_start_397263.png

General Structure at the Start of Filter Layer Overview – Periphery

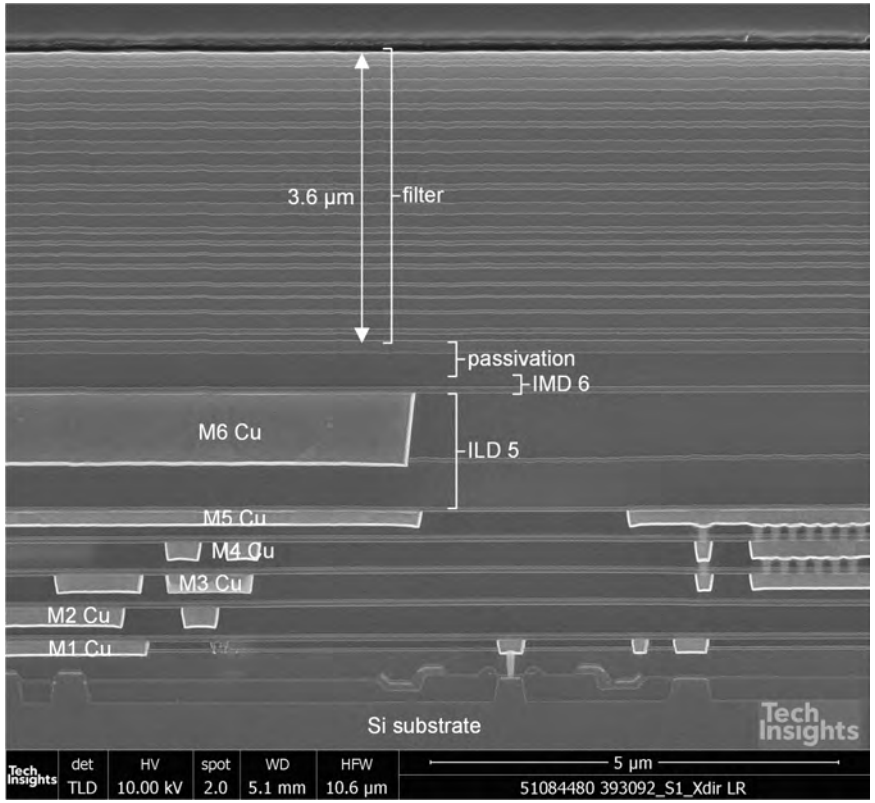
General Structure – Periphery

- The left image is a SEM cross section close-up showing the start of the filter layer formed over the SPAD array.
- The right image shows the periphery region under the filter layer, before the start of the SPAD array.



556_General_Structure_393092.png

General Structure at the Start of Filter Layer Close-Up – Periphery

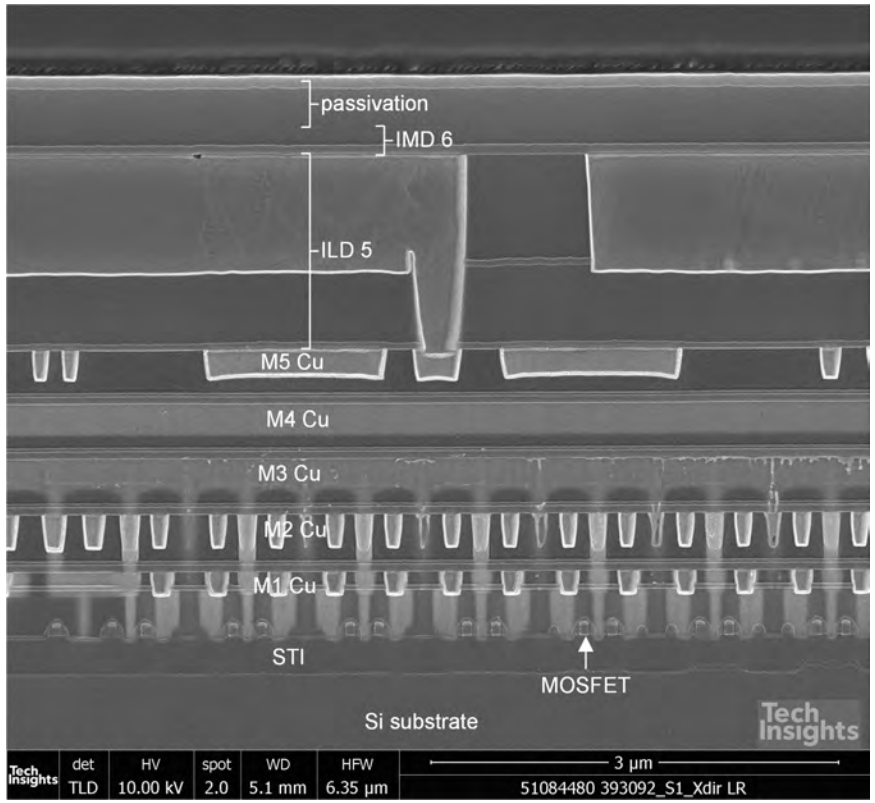


550_General_Structure_393092.png

General Structure Near the Start of the SPAD Array – Periphery

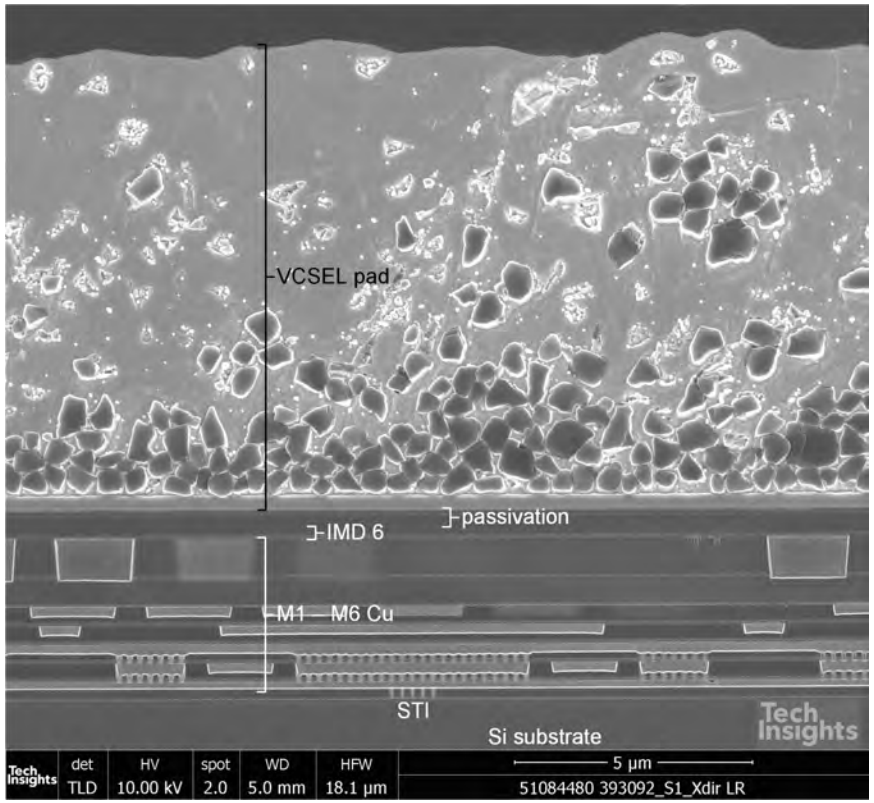
General Structure – Periphery

- The left image shows the SRAM region.
- The right image shows the VCSEL pad region formed over the SPAD die during the assembly process.



569_SRAM_393092.png

General Structure at the SRAM Region – Periphery

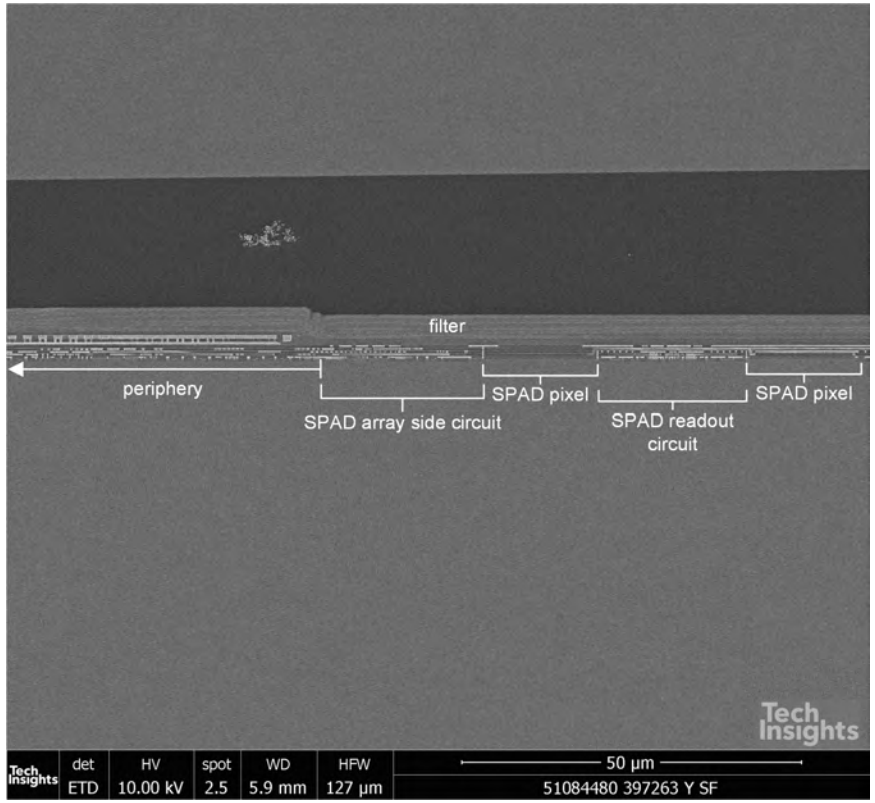


653_Region_Bellow_VCSEL_Die_393092.png

General Structure at the VCSEL Region – Periphery

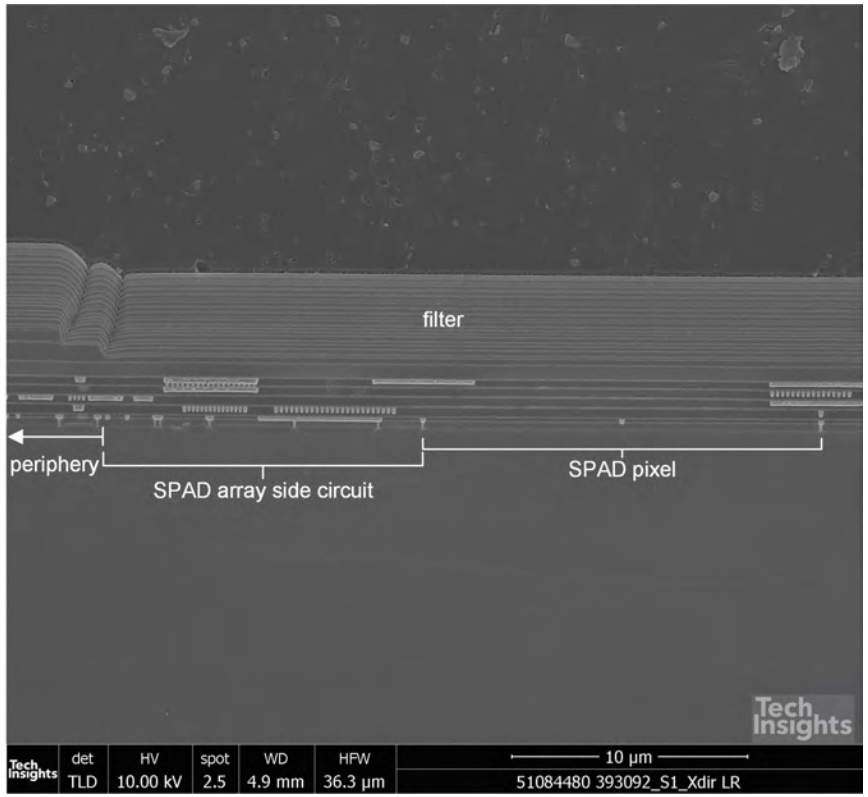
General Structure – SPAD Array X-Direction

- SEM cross section images in the X-direction showing the general structure at the transition from periphery to SPAD array on the left side



018_periphery_to_array_397263.png

Transition from Periphery to SPAD Array Overview

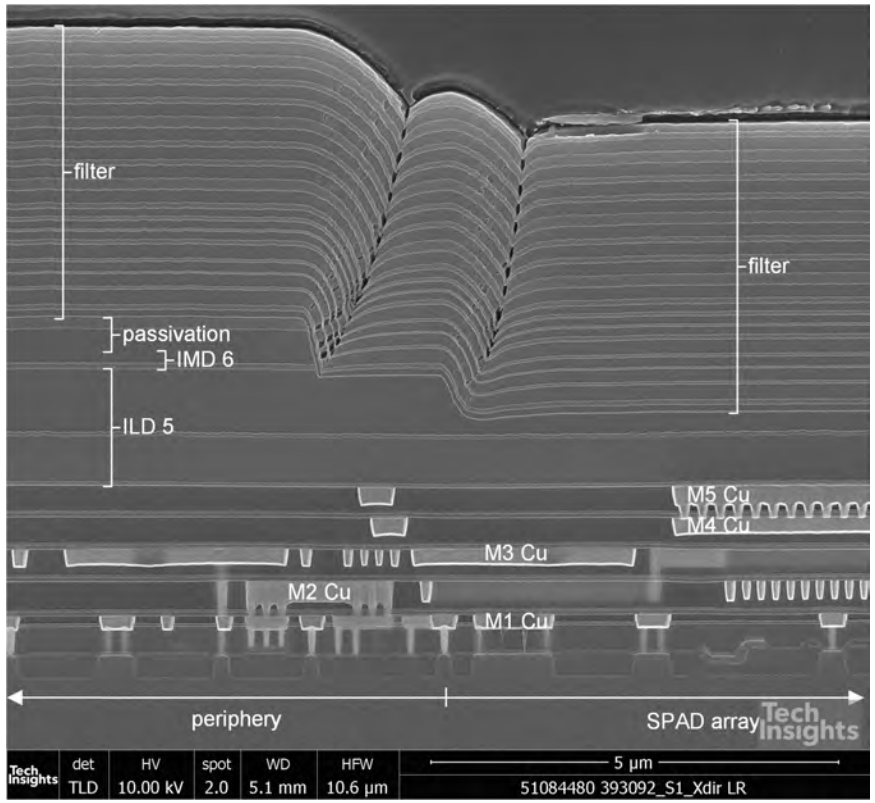


909_Edge_of_Active_Array_393092.png

Start of SPAD Array General Structure Overview

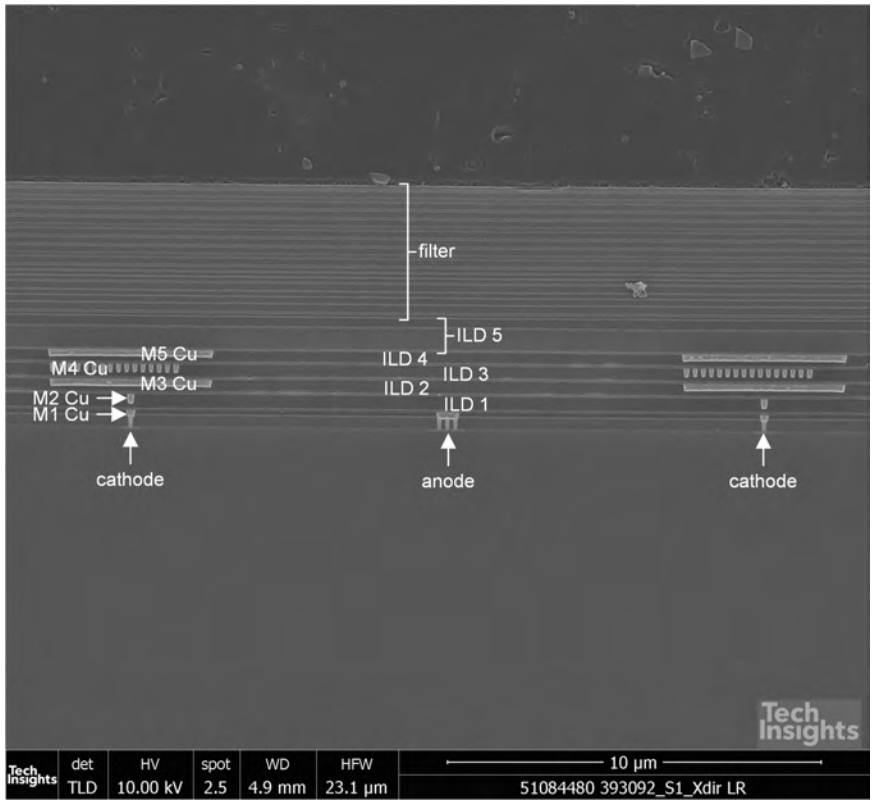
General Structure – SPAD Array X-Direction

- SEM cross section images in the X-direction showing a close-up of the left side transition from periphery to SPAD array, and overview of the SPAD pixel.
- At the transition from periphery to pixel array, a step in the upper dielectric layers is formed by the etching of passivation, IMD 6 and ILD 5.4 layers
- In the X-direction, the SPAD array five metal interconnects and comprises rows of SPAD pixels interleaved with rows of SPAD readout circuitry.



547_End_of_Active_SPAD_Array_between_Slice_B_C_393092.png

Transition from Periphery to SPAD Array Close-Up

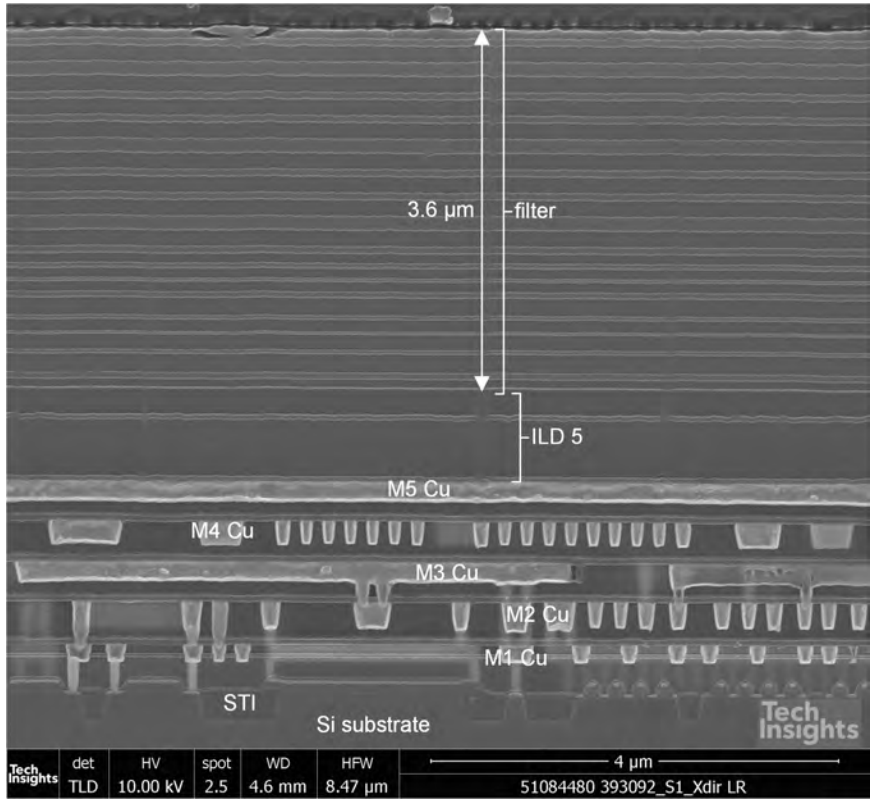


903_Active_Array_Centre_of_SPAD_Pixel_SliceA_393092.png

SPAD Pixel Overview

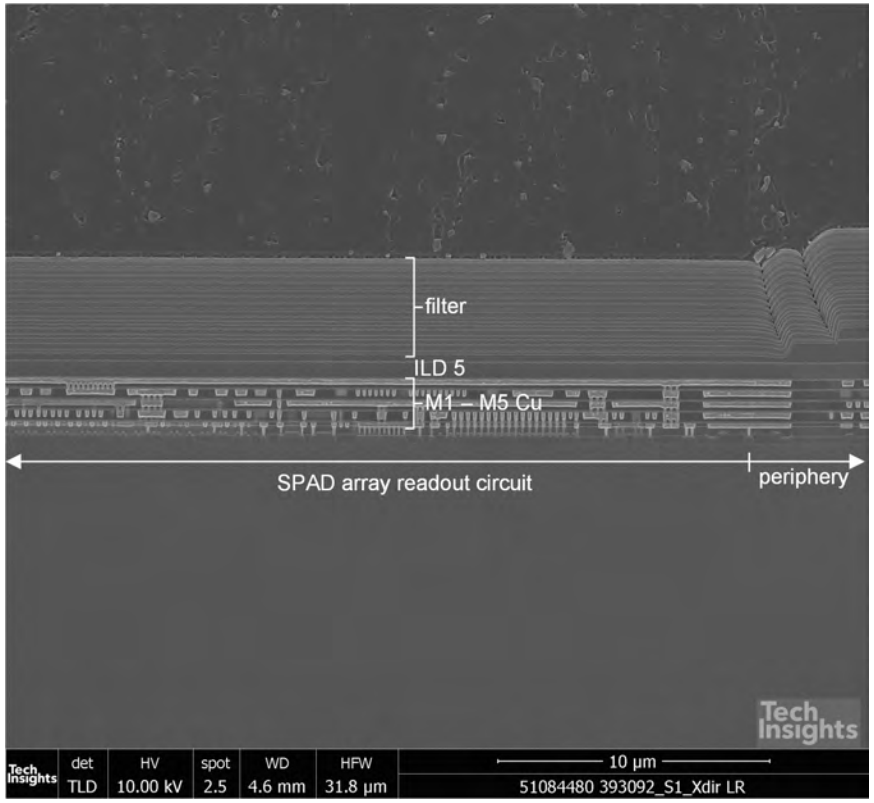
General Structure – SPAD Array X-Direction

- SEM cross section images in the X-direction showing the SPAD array readout circuitry and the right-side transition from periphery to SPAD array
- The SPAD array uses five metal interconnect layers, and the filter layer is formed on ILD 5-4.
- At the transition from periphery to pixel array, a step in the upper dielectric layers is formed by the etching of passivation, IMD 6 and ILD 5.4 layers



811_Active_SPAD_393092.png

SPAD Array Readout Circuitry Overview

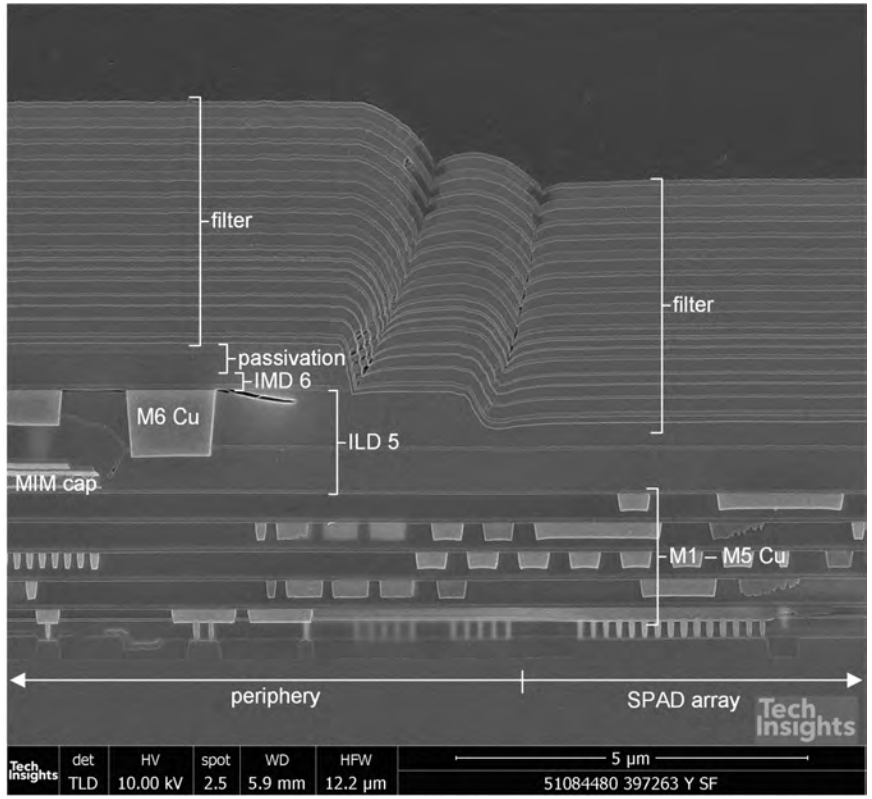


806_Active_SPAD_393092.png

Transition from SPAD Array to Periphery Overview

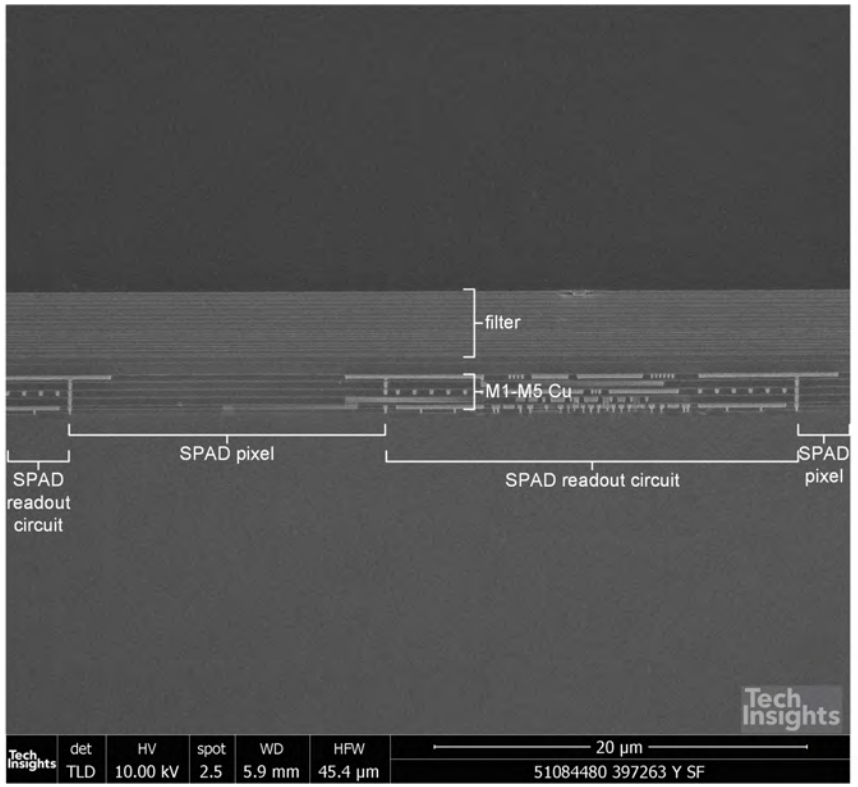
General Structure – SPAD Array Y-Direction

- SEM cross section images in the Y-direction showing a close-up of the transition from periphery to SPAD array, and overview of the SPAD array.
- At the transition from periphery to pixel array, a step in the upper dielectric layers is formed by the etching of passivation, IMD 6 and ILD 5.4 layers
- In the Y-direction, the SPAD array comprises SPAD pixel interleaved with the SPAD readout circuitry.



019_periphery_to_array_397263.png

Transition from Periphery to SPAD Array Close-Up

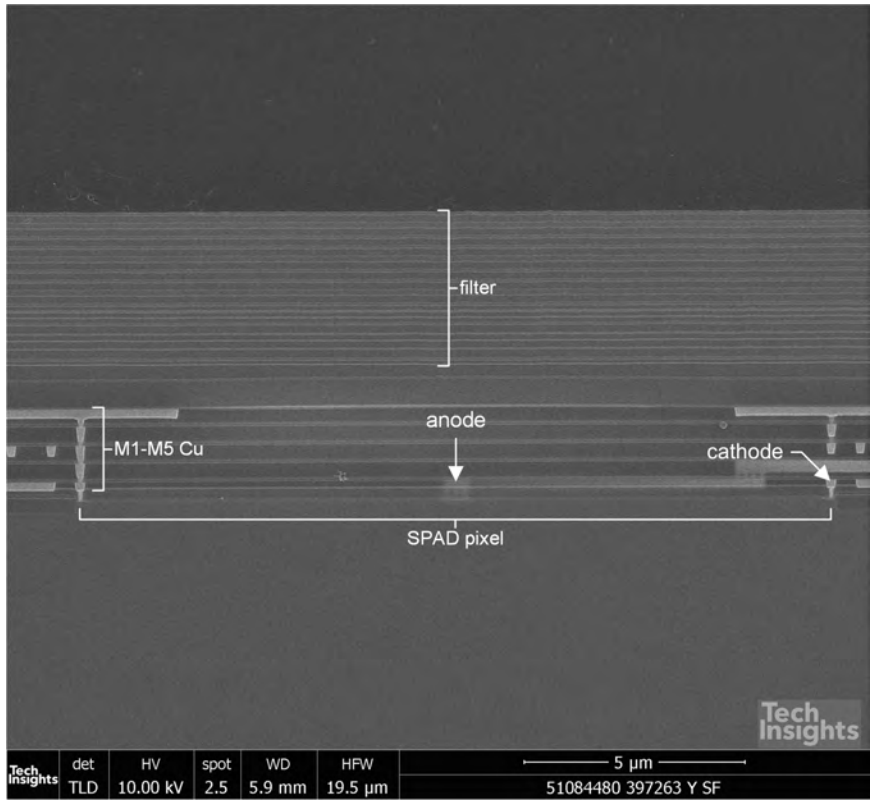


026_array_SPAD_locD_midpixel_397263.png

SPAD Pixel and SPAD Readout Circuit Overview

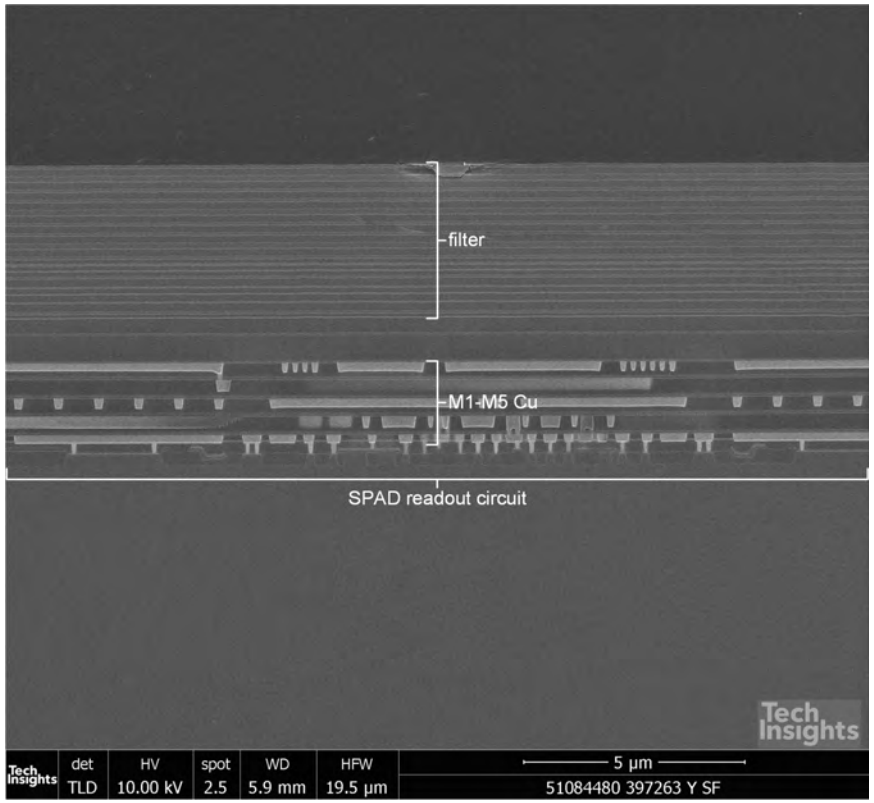
General Structure – SPAD Array Y-Direction

- SEM cross section images in the Y-direction showing the overview of the SPAD pixel and SPAD readout circuit.
- The SPAD array uses five metal interconnect layers, and the filter layer is formed on ILD 5-4.



027_array_SPAD_locD_midpixel_397263.png

SPAD Pixel Overview

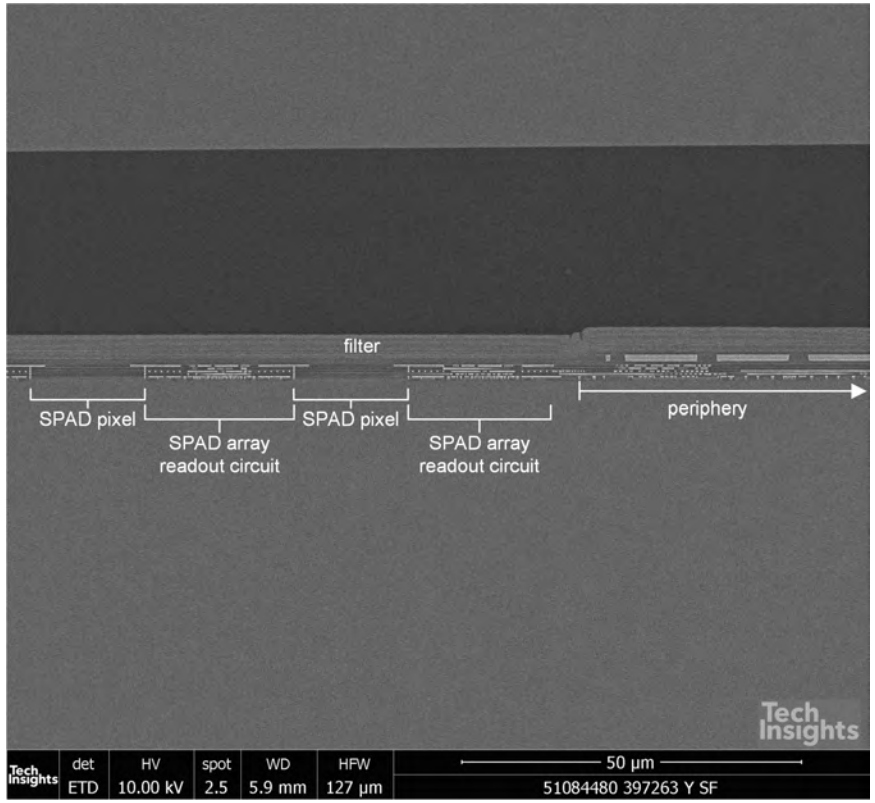


028_array_SPAD_locD_midpixel_circuitry_397263.png

SPAD Readout Circuit Overview

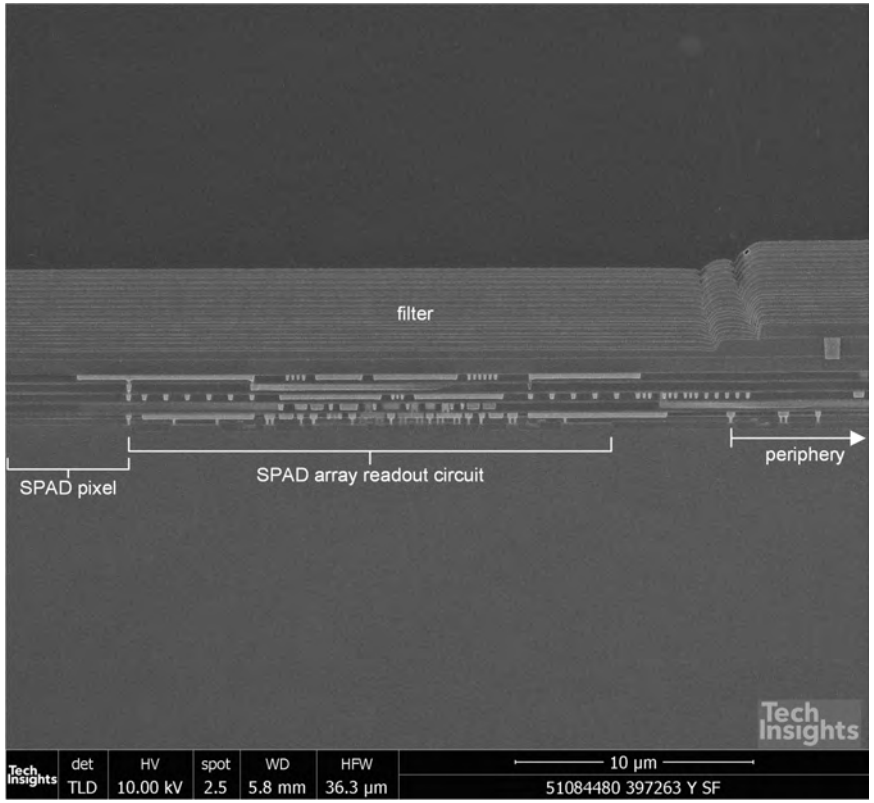
General Structure – SPAD Array Y-Direction

- SEM cross section images in the Y-direction showing the transition from SPAD array to periphery



046_periphery_to_array_397263.png

Transition from SPAD Array to Periphery Overview

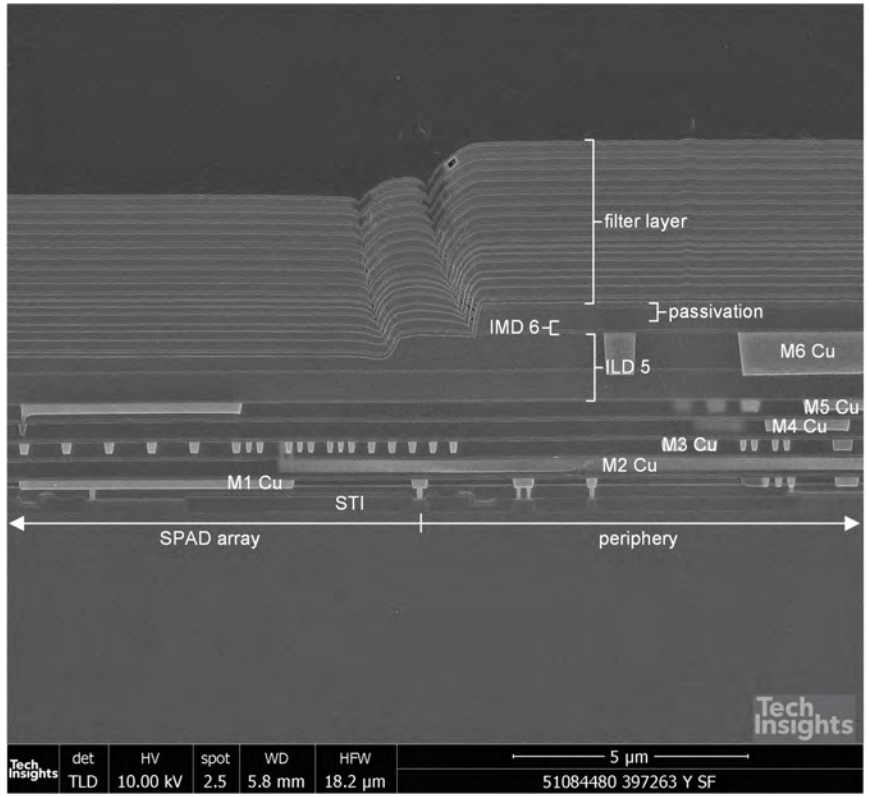


045_periphery_to_array_397263.png

Transition from SPAD Array to Periphery Overview

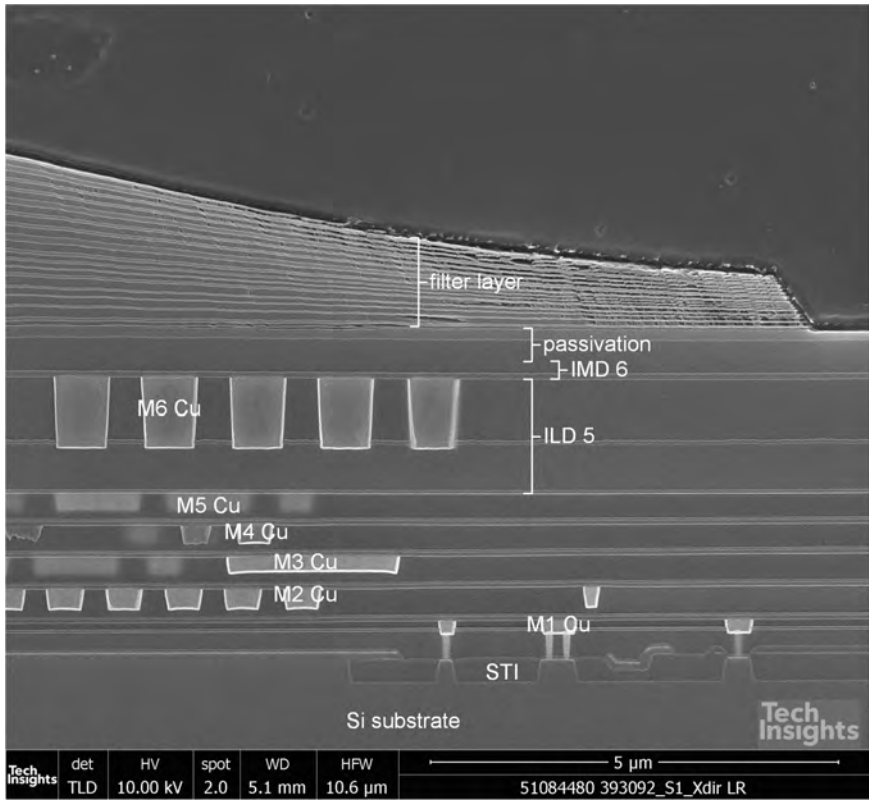
General Structure – SPAD Array Y-Direction

- SEM cross section images in the Y-direction showing the transition from SPAD array to periphery, and the end of the filter layer at the bottom side of the SPAD array.



047_periphery_to_array_397263.png

Transition from SPAD Array to Periphery Close-Up



507_Start_of_Active_SPAD_Array_Coating_393092.png

End of Filter Layer on the Bottom Side of SPAD Array

d-TOF Die P- and N-Type Regions

Tech Insights

P- and N-Type Regions – Vertical Dimensions

Feature	Dimension (µm)
I/O P-well	1.3(b)
I/O N-well	4.5(b)
I/O NMOS S/D	0.22(b)
Logic P-well depth	1.5(b)
Logic N-well depth	3.5(a)
SPAD readout circuitry P-well depth	1.5(b)
SPAD readout circuitry N-well depth	4.5(b)
SPAD cathode depth	4.5(b)
SPAD anode depth	0.72(b)

(a) Dimensions based on the SRP profiles
(b) Dimensions based on the SCM images
(c) Dimensions based on the SIMS profile

P- and N-Type Regions – Doping Levels

Location	Feature	Doping Type / Dopant	Doping (cm^{-3})
–	Si substrate	P-type/11B	1.2×10^{15} (a, c)
Logic	Shallow N-well	N-type/31P	2.4×10^{17} (c)
Logic	Deep N-well	N-type/31P	6×10^{16} (a, c)
Logic	P-well	P-type/11B	3×10^{17} (c)
Logic	PMOS S/D	P-type/11B	2×10^{18} (c)
Logic	NMOS S/D	N-type/31P	1×10^{18} (c)
SPAD readout circuitry	PMOS S/D	P-type/11B	3×10^{18} (c)
SPAD readout circuitry	NMOS S/D	N-type/31P	2×10^{18} (c)
SPAD readout circuitry	N-well	N-type/31P	$1 \times 10^{15} – 6 \times 10^{16}$ (c)
SPAD readout circuitry	P-well	P-type/11B	3×10^{17} (c)
SPAD	Lower doped cathode bottom	N-type/31P	$1 \times 10^{15} – 6 \times 10^{16}$ (c)
SPAD	Higher doped cathode top	N-type/31P	6×10^{16} (c)
SPAD	Anode surface	P-type/11B	1.4×10^{19} (c)
SPAD	Anode contact	P-type/11B	3×10^{18} (c)
SPAD	Anode body	P-type/11B	3×10^{17} (c)
SPAD	Anode guard ring	P-type/10B	6×10^{17} (c)

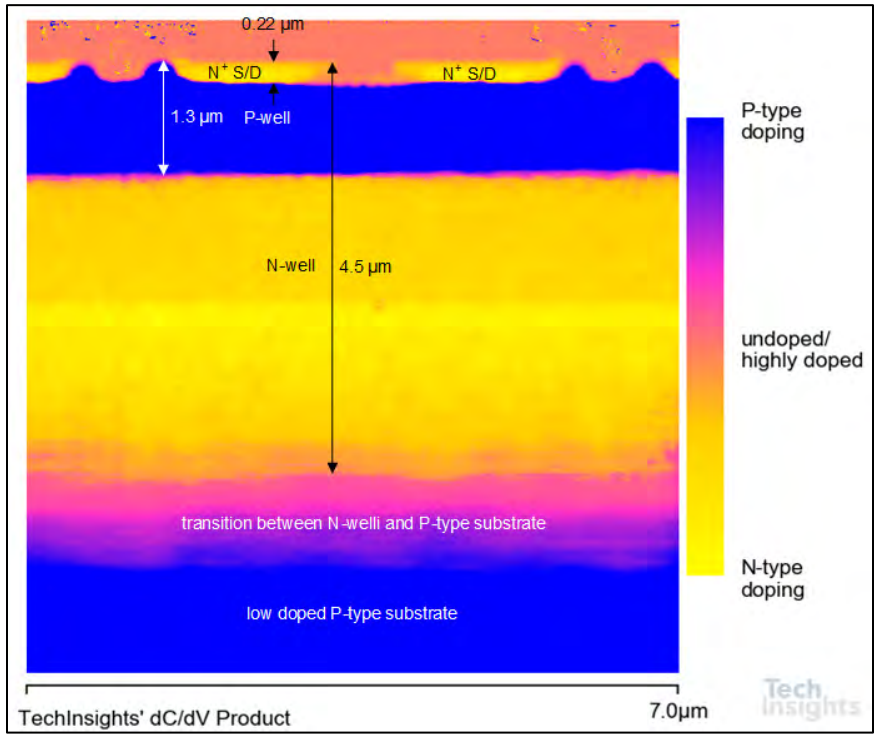
(a) Doping concentration based on the SRP profiles
(b) Doping concentration based on the SCM images
(c) Doping concentration based on the SIMS profile

P- and N-Type Regions Analysis

- SIMS and SPM (SCM/SMIM) analyses were carried out to investigate the d-TOF N- and P-type wells, as well as the pixel doping profiles. The starting material wafer doping type could not be established through these analyses because the d-TOF wafer thinning has removed the bulk of the substrate.
- Generally, SCM images give a yellow color mapping for N-type material, a purple/blue color mapping for P-type material, and a pink color mapping for highly doped and undoped materials. The colors may vary slightly, however, due to adjustments in the scan settings, SCM tip wear, and localized structures present in the scanning region, such as W B-DTI fill.
- SMIM is a near-field technique that detects reflections in a 3 GHz microwave system, which includes the interaction between a shielded atomic force microscopy (AFM) tip and the sample under test. This is much like a standard microwave impedance measurement, but the small tip of the AFM allows for high spatial resolution and rastering of the probe to create a map of local electrical properties. The SMIM-C image is the reactive part of the impedance interface between the AFM tip and the cross-sectioned sample. The contrast in the image is proportional to the capacitance of the sample under inspection. The brighter green is related to a higher dopant concentration, while the darker green/black is related to a lower dopant concentration.

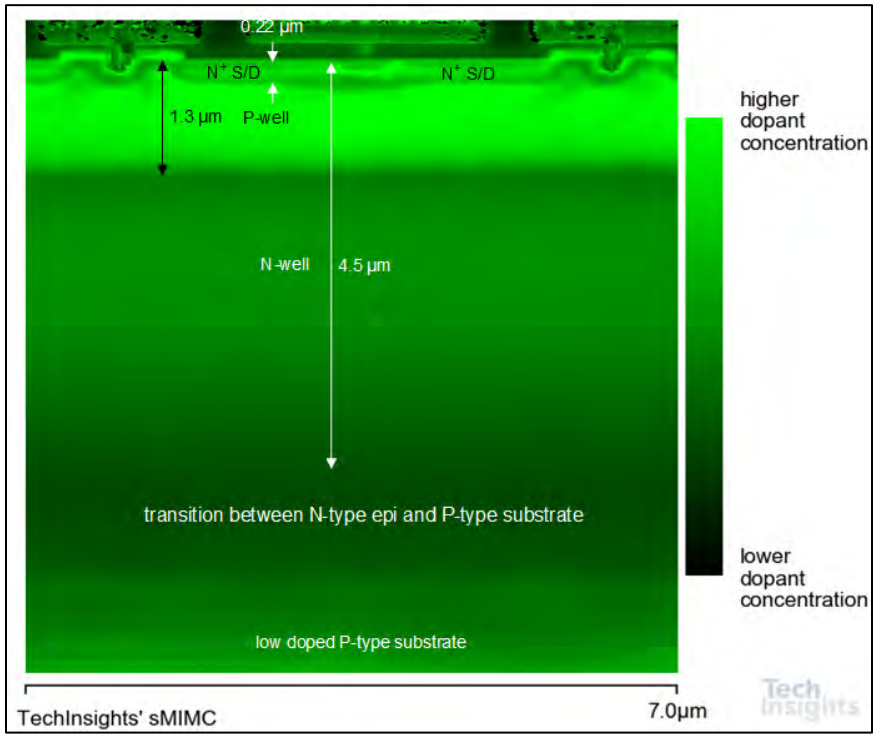
P- and N-Type Regions I/O – SPM

- SCM and SMIM-C cross section images in the I/O region
- In the I/O region, there is a 4.5 µm deep N-well, and a 1.3 µm deep P-well.
- The NMOS transistor S/D regions are 0.22 µm deep.
- The substrate is low doped P-type



IO_under_bondpad_030922184123_PRODUCT_FRW_7.0u_512p_393092.png

I/O Region Wells – SCM

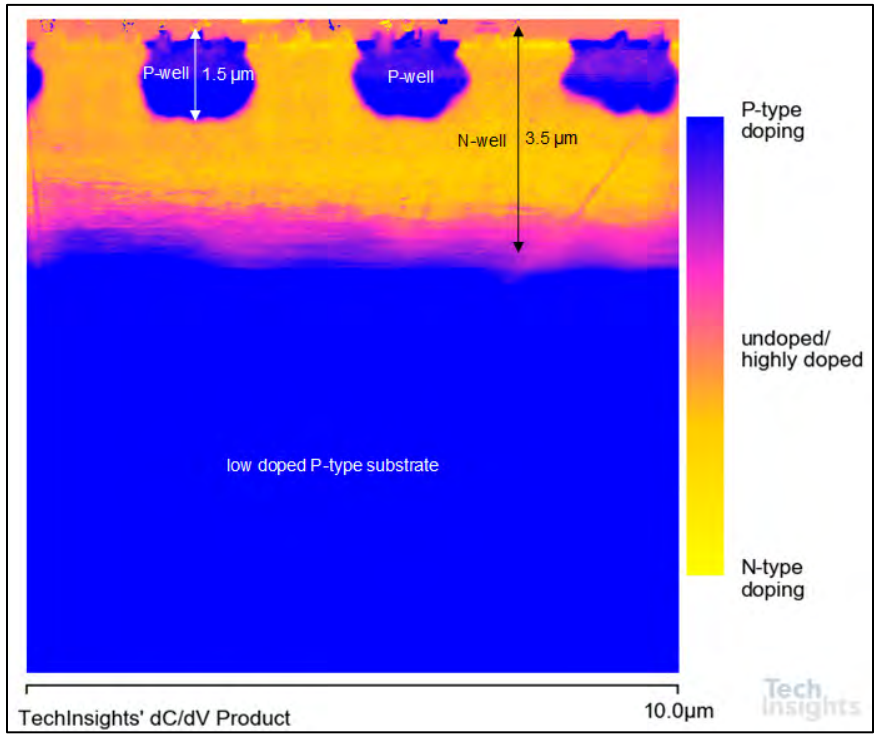


IO_under_bondpad_030922184123_SMIMC_FRW_7.0u_512p_393092.png

I/O Region Wells – SMIM-C

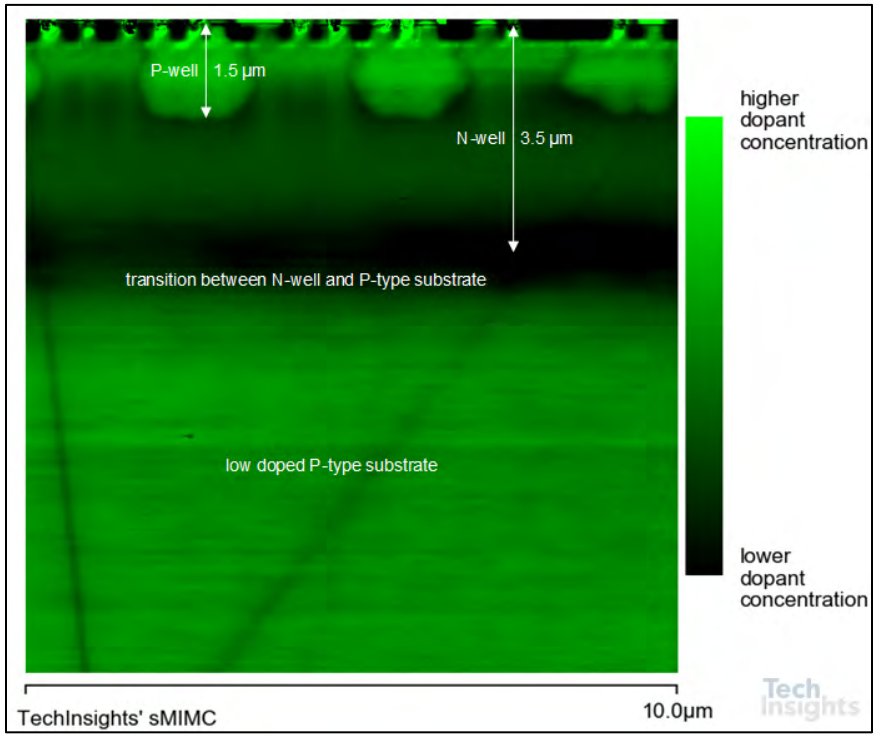
P- and N-Type Regions Logic – SPM

- SCM and SMIM-C cross section images in the logic region
- In the logic region, there is a 1.5 µm deep P-well, and a 3.5 µm deep N-well with a lower doped region at the bottom.
- The substrate is low doped P-type.



Logic_030922145952_PRODUCT_FRW_10.0u_512p_393092.png

Logic Region Wells – SCM

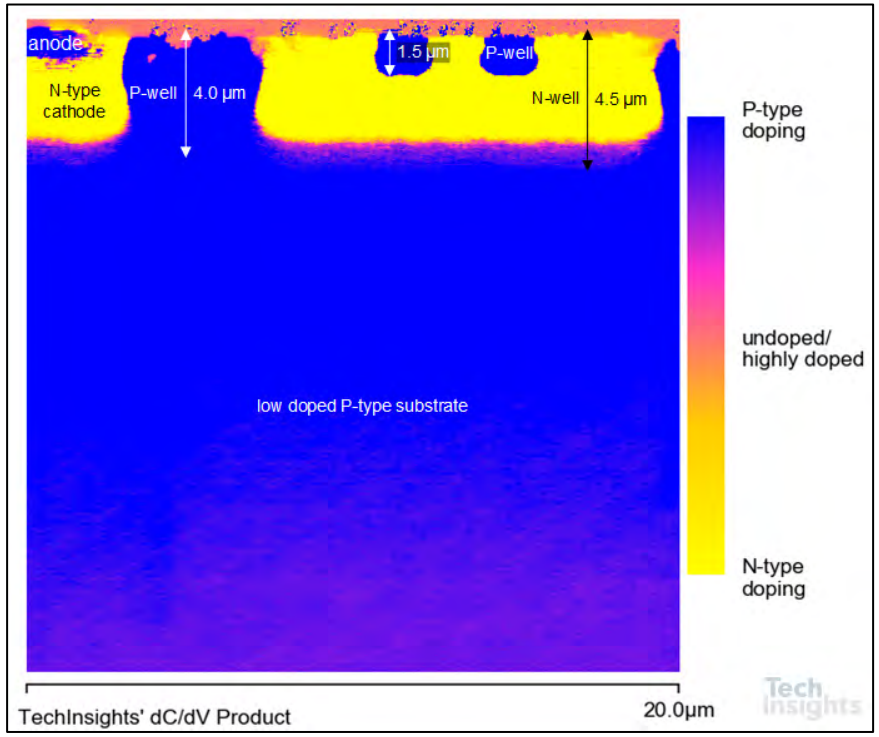


Logic_030922145952_SMIMC_FRW_10.0u_512p_393092.png

Logic Region Wells – SMIM-C

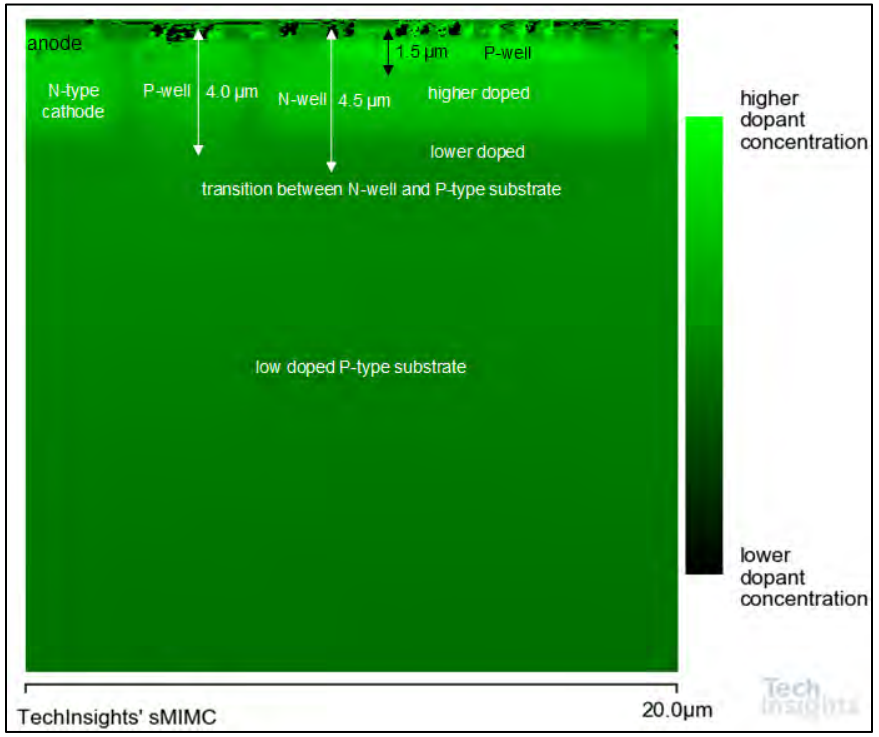
P- and N-Type Regions SPAD Readout Circuit – SPM

- SCM and SMIM-C cross section images in the SPAD readout circuit region
- In the SPAD readout circuit region, there is a 1.5 µm deep P-well, and a 4.5 µm deep N-well with a lower doped region at the bottom.
- Between the readout circuit N-well and the SPAD, there is a 4.0 µm deep P-well
- The substrate is low doped P-type.



locD_transistors_031122190115_PRODUCT_FRW_20.0u_512p_397263.png

SPAD Readout Circuit Region Wells – SCM

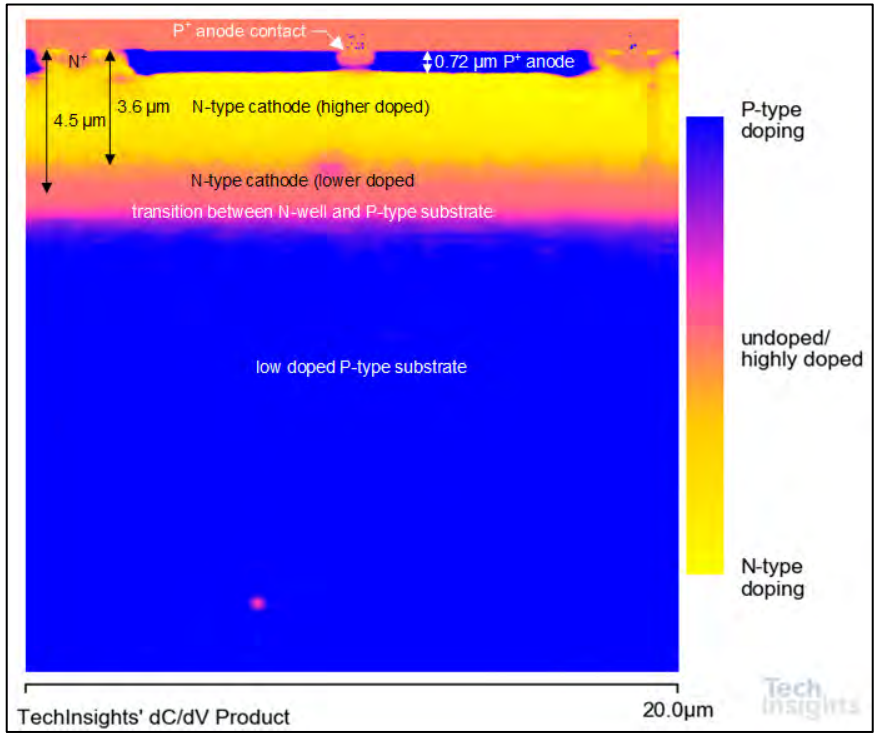


locD_transistors_031122190115_SMIMC_FRW_20.0u_512p_397263.png

SPAD Readout Circuit Region Wells – SMIM-C

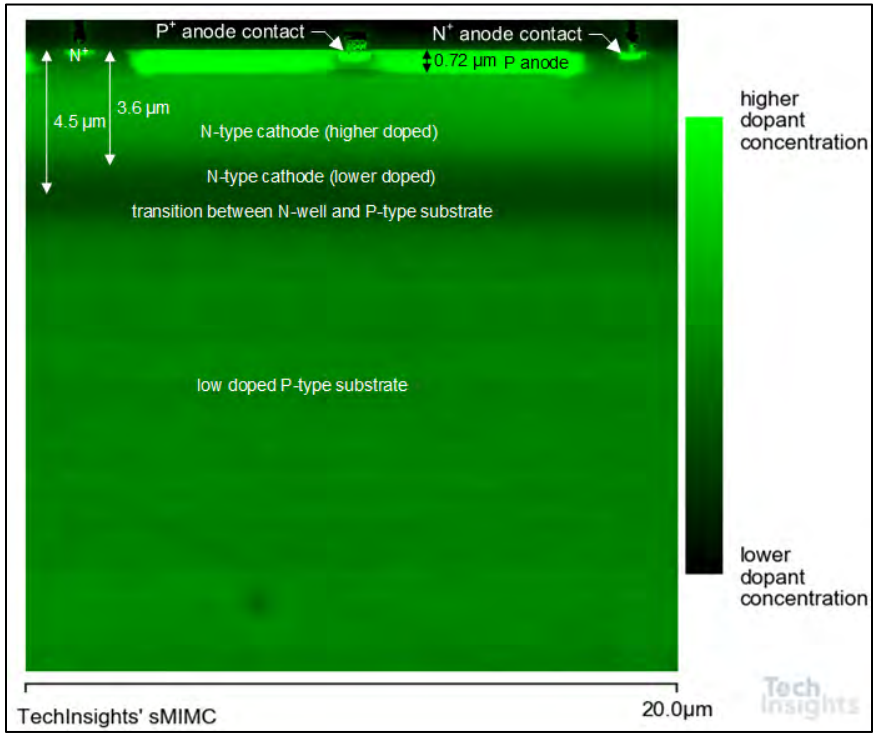
P- and N-Type Regions SPAD Pixel – SPM

- SCM and SMIM-C cross section images through the center of the SPAD
- The anode is 0.72 µm deep high doped P-type.
- The cathode is ~4.5 µm deep, has an ~3.6 µm deep higher doped upper region, and an ~0.90 µm deep lesser doped lower region.



Midpixel_030822164545_PRODUCT_FRW_20.0u_512p_393092.png

SPAD Overview – SCM

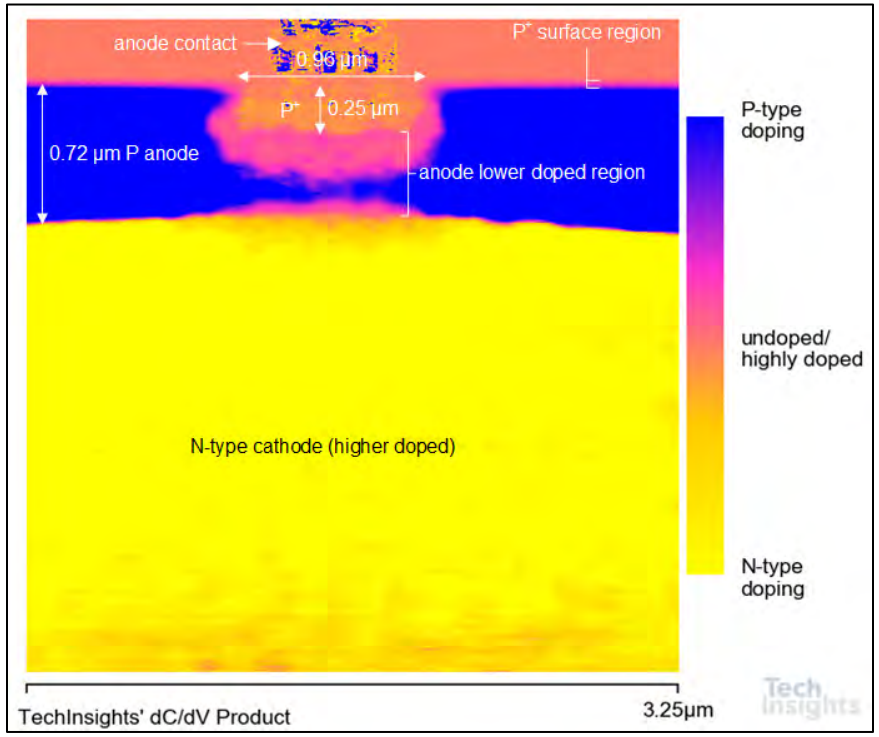


Midpixel_030822164545_SMIMC_FRW_20.0u_512p_393092.png

SPAD Overview – SMIM-C

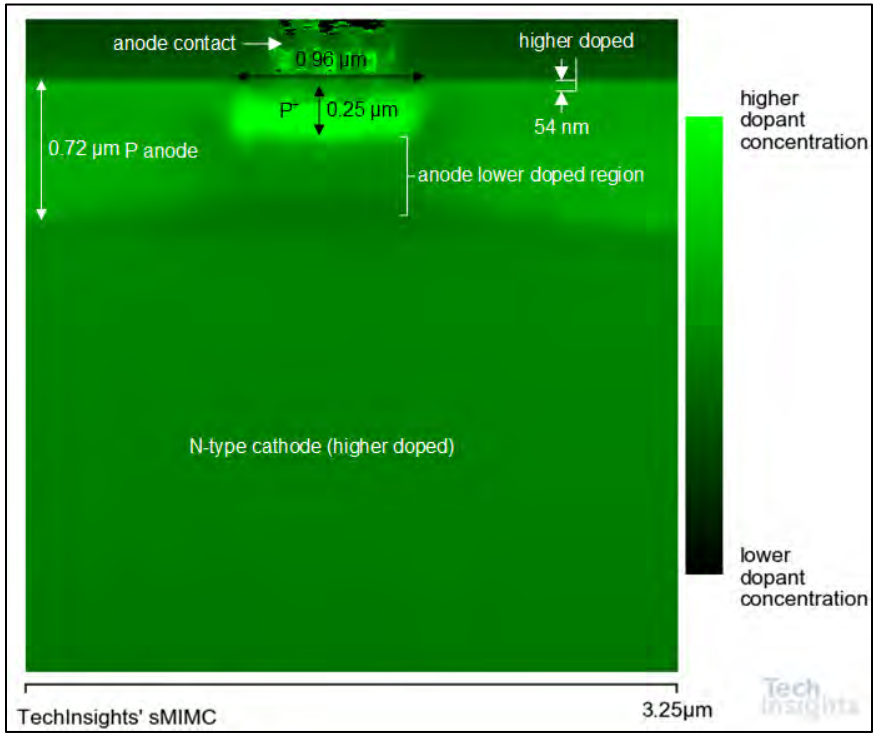
P- and N-Type Regions SPAD Pixel – SPM

- SCM and SMIM-C cross section close-up images of the SPAD anode contact.
- The anode contact is 0.25 µm deep P^+ region, with a lower doped P-type region between the P^+ region and the N-type cathode.
- An ~54 nm deep surface region of the anode is higher doped than the anode body.



Midpixel_030822191807_PRODUCT_FRW_3.25u_512p_393092.png

Anode Contact Detail – SCM

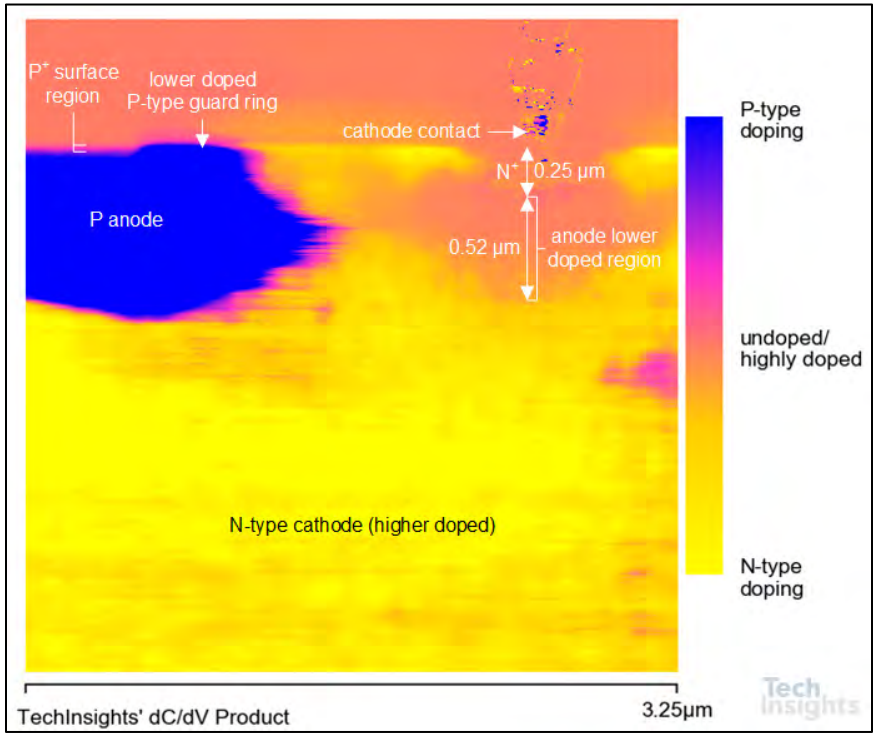


Midpixel_030822191807_SMIMC_FRW_3.25u_512p_393092.png

Anode Contact Detail – SMIM-C

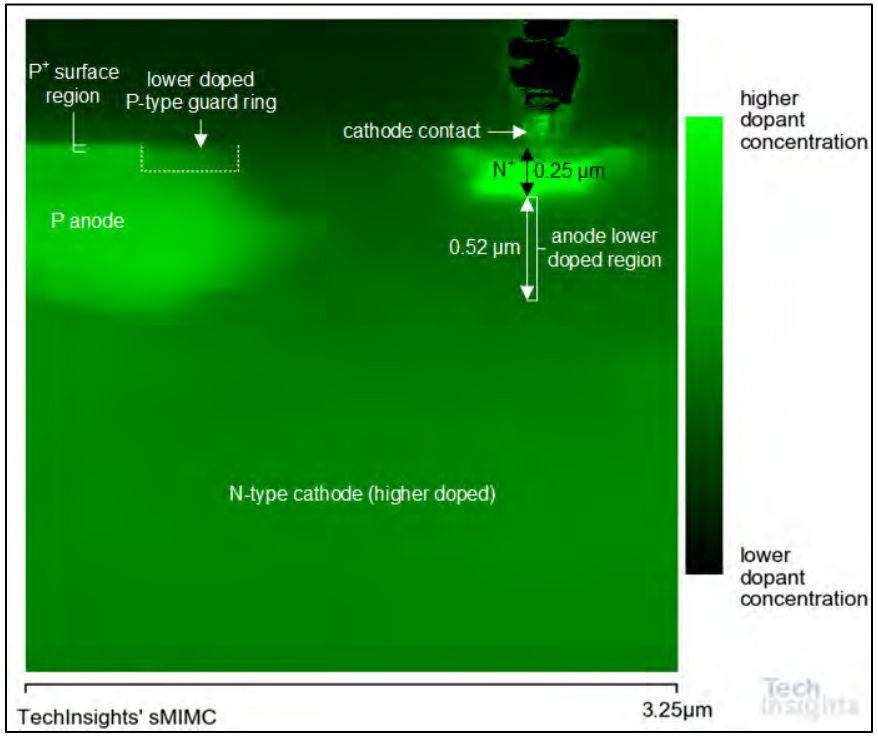
P- and N-Type Regions SPAD Pixel – SPM

- SCM and SMIM-C cross section close-up images of the SPAD cathode contact.
- The cathode contact is 0.25 µm deep N^+ region, with a lower doped N-type region below and on the sides.
- At the top edge of the anode there is a lower doped P-type guard ring.



Midpixel_030822185110_PRODUCT_FRW_3.25u_512p_393092.png

Cathode Contact Detail - SCM



Midpixel_030822185110_SMIMC_FRW_3.25u_512p_393092.png

Cathode Contact Detail - SMIM-C

P- and N-Type Regions – SIMS

- SIMS analysis was performed in the d-TOF pixel array and periphery.
- The sample was prepared by removing the front layers down to the Si surface.
- The analysis locations are annotated on the optical image of the SIMS sample on page 21.
- The SIMS crater for boron (B) analysis is 100 × 100 µm, and 80 × 80 µm for the remaining elements.
- The primary ion sources include O2+, typically used for the detection of electropositive species, and Cs+ for electronegative species.

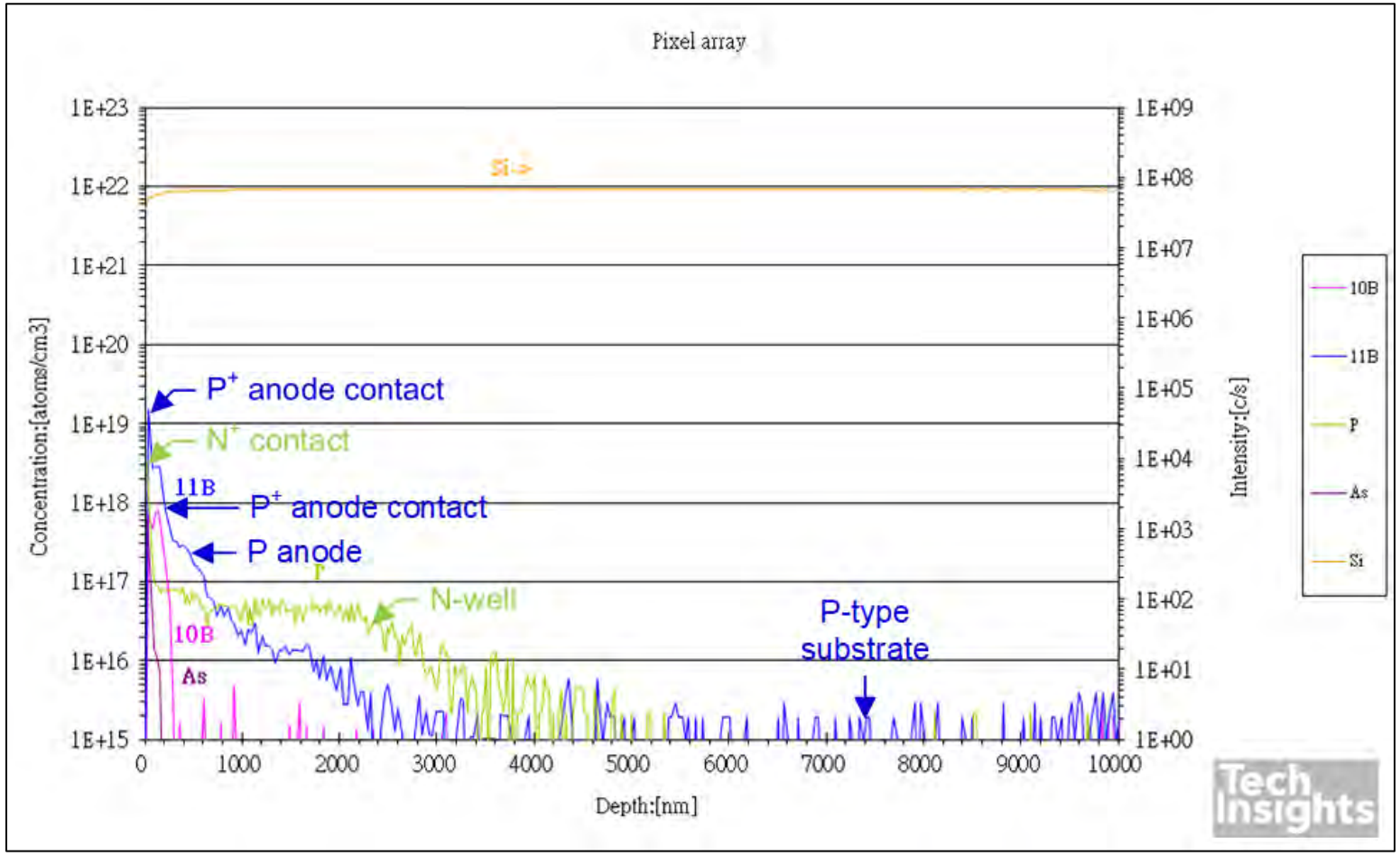
Note: The SIMS doping concentrations are not corrected for the corresponding areas of each pixel array feature.

P- and N-Type Doping Profiles SPAD Array – SIMS

The SIMS profile showing the doping concentration in the pixel array is displayed on page 49.

- 11B (boron) doping at the surface has a doping concentration peak of 1.4×10^{19} cm^{-3}, which likely corresponds to the P^+ anode region at the surface. Then 11B has a second doping concentration peak of 3×10^{18} cm^{-3}, which likely corresponds to the P^+ anode contact region and maybe the readout circuit PMOS S/D regions. A third doping concentration peak of 3×10^{17} cm^{-3} is observed, which likely corresponds to the P anode body and readout circuit P-well. Finally, 11B doping concentration gradually decreases reaching about 1.5×10^{15} cm^{-3}, around a depth of 3 µm, which corresponds to the P-type Si substrate.
- 10B (boron) doping near the surface has a doping concentration peak of 6×10^{17} cm^{-3}, which likely corresponds to the lower doped guard ring formed around the P-type anode. Below a depth of 0.15 µm, 10B doping concentration falls below 1×10^{15} cm^{-3}.
- Phosphorus (31P) has a peak doping concentration of about 2×10^{18} cm^{-3} at the Si surface, which likely corresponds to the N^+ contact region and NMOS S/D regions. Then 31P doping concentration sharply falls reaching an average of 6×10^{16} cm^{-3}, which likely corresponds to the top higher doped portion of the cathode region and readout circuit N-well. At a depth of 2.2 µm, 31P doping concentration starts gradually decreasing, reaching about 1×10^{15} cm^{-3} at a depth of 4.5 µm, which likely corresponds to bottom lower doped cathode region.
- Arsenic (75As) near the surface has a doping concentration of about 3×10^{16} cm^{-3}, which could be also corresponds to the low doped cathode region surrounding the cathode contact. Below a depth of 0.10 µm 75As doping concentration fall below 1×10^{15} cm^{-3}.

P- and N-Type Doping Profiles SPAD Array – SIMS



SIMS_Analysis_SPAD_Array_Doping_Profiles.png

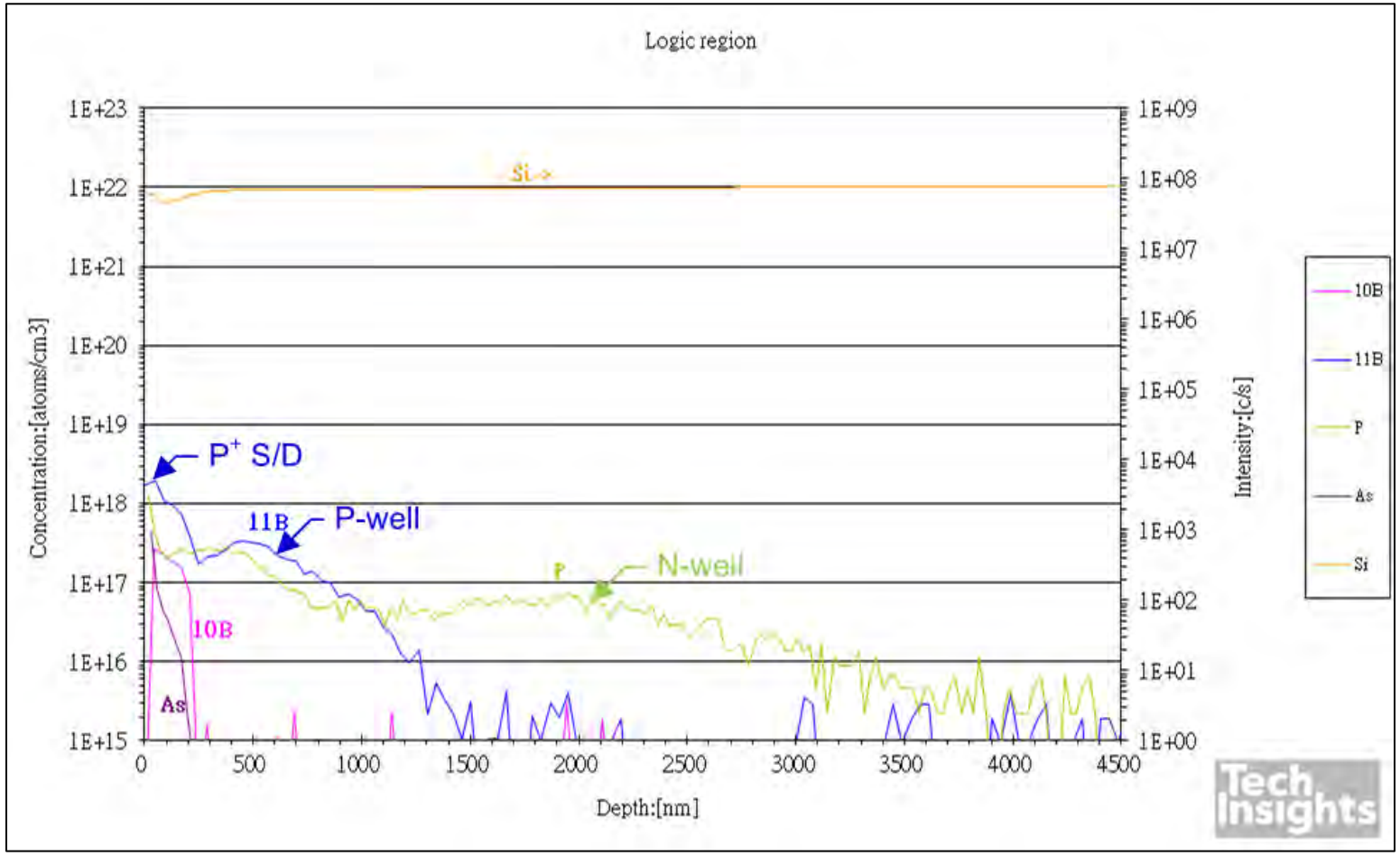
SPAD Array Doping Profiles - SIMS

P- and N-Type Doping Profiles Logic – SIMS

The SIMS profile showing the doping concentration in the periphery region 1 (logic) is displayed on page 51.

- 11B doping concentration at the Si surface peaks at 2 × 10^{18} cm^{-3}, which likely corresponds to the P-type S/D regions. Then 11B at a depth of 0.5 µm has a second peak doping concentration of 3.0 × 10^{17} cm^{-3}, which likely corresponds to the P-well. After, 11B gradually decreases, reaching a doping concentration of 1 × 10^{15} cm^{-3} at a depth of 1.5 µm, which corresponds to the doping concentration of the P-type Si substrate.
- 10B is also present near the Si surface, with a peak doping concentration of about 2.0 × 10^{17} cm^{-3}, which may also likely correspond to the P-type S/D regions.
- 31P doping concentration at the Si surface peaks at 1.0 × 10^{18} cm^{-3}, which likely corresponds to the N-type S/D regions. Then 31P doping concentration sharply decreases to 2.4 × 10^{17} cm^{-3}, which likely corresponds to the upper higher doped portion of the N-well. Next, at a depth of 0.50 µm, 31P doping concentration gradually decreases reaching an average of 6 × 10^{16} cm^{-3}, which likely corresponds to the middle portion of the N-well. Finally, at a depth of 2.2 µm, 31P doping concentration gradually decreases to reach 1.0 × 10^{15} cm^{-3}, at a depth of approximately 4.0 µm. Below 4.0 µm, 31P signal is only noise.
- 75As is only present near the Si surface, with a peak doping concentration of about 4 × 10^{17} cm^{-3}, which may likely correspond to the N-type S/D regions.

P- and N-Type Doping Profiles Logic – SIMS



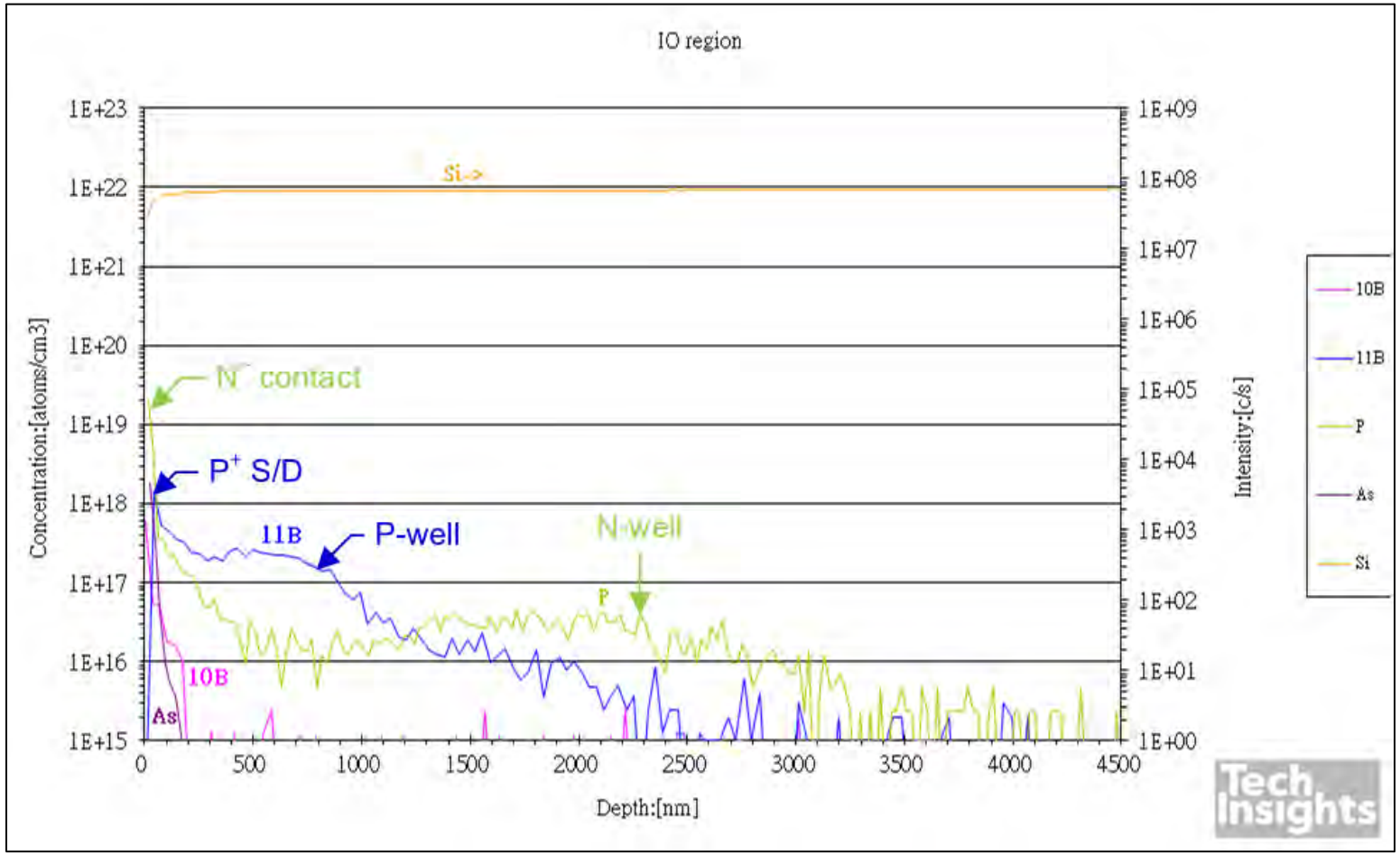
SIMS_Analysis_Logic_Region_Doping_Profiles.png

Logic Region Doping Profile – SIMS

P- and N-Type Doping Profiles I/O – SIMS

- The SIMS profile showing the doping concentration in the periphery region 2 (I/O) is displayed on page 53.
- 11B doping concentration at the Si surface peaks at 1.2 × 10^{18} cm^{-3}, which likely corresponds to the P-type S/D regions. Then 11B doping concentration decreases reaching an average of 2 × 10^{17} cm^{-3}, at a depth of about 0.20 µm, which likely corresponds to the P-well region. Finally, at a depth of about 0.70 µm 11B doping concentration gradually decreases to reach 1.0 × 10^{15} cm^{-3}, at a depth of approximately 2.5 µm, which corresponds to the P-type Si substrate.
- 10B is also present near the Si surface, with a peak doping concentration of about 6 × 10^{17} cm^{-3}, which may also likely correspond to the P-type S/D regions.
- 31P doping concentration at the Si surface peaks at 2.0 × 10^{19} cm^{-3}, which likely corresponds to the N-type S/D regions. Then 31P doping concentration sharply decreases reaching an average doping concentration of 2.0 × 10^{16} cm^{-3}, at a depth of about 0.50 µm, then at a depth of about 1.3 µm, 31P doping concentration increases slightly to an average of about 4 × 10^{16} cm^{-3}, which likely corresponds to the N-well. Then at a depth of 2.3 µm, 31P doping concentration gradually decreases to reach 1 × 10^{15} cm^{-3}, at a depth of approximately 4.5 µm. Below 4.5 µm, 31P signal is only noise.
- 75As is only present near the Si surface, with a peak doping concentration of about 2 × 10^{18} cm^{-3}, which may likely correspond to the N-type S/D regions.

P- and N-Type Doping Profiles I/O – SIMS

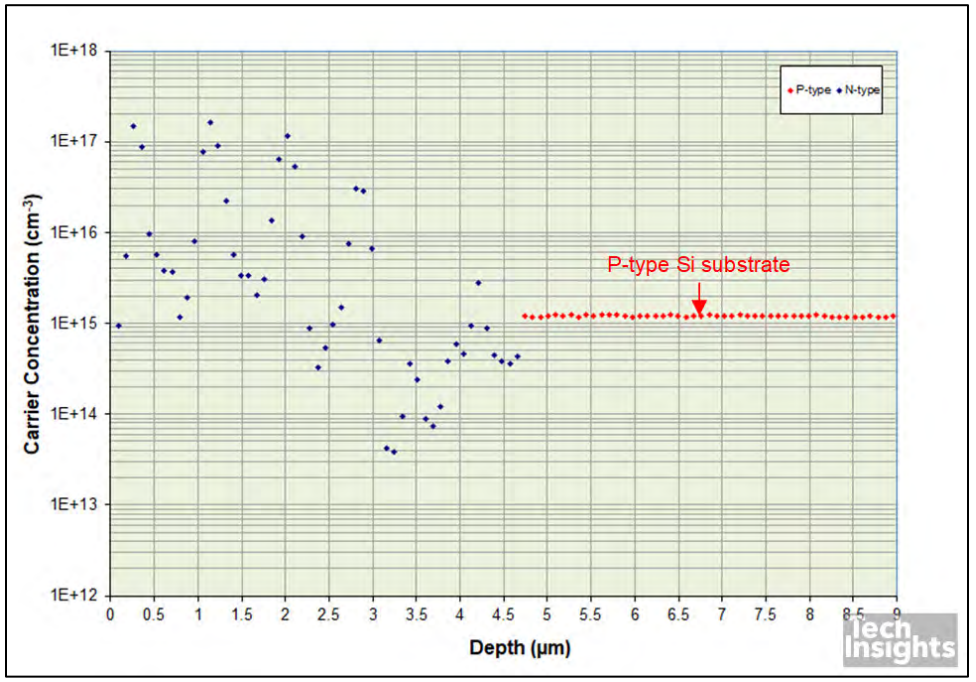


SIMS_Analysis_IO_Region_Doping_Profiles.png

I/O Region Doping Profile – SIMS

P- and N-Type Doping Profiles SPAD Array – SRP

- SRP analysis was performed in the d-TOF SPAD array, logic, and periphery regions. The sample was prepared by removing the front layers down to the Si surface. The analysis locations are shown on the optical image on page 21.
- SRP analysis in the SPAD array; Probe Load 5, bevel angle 0.02195 <100> Si X-step 4 µm. It was not possible to obtain the pixel array doping concentration near the surface up to a depth of 4.5 µm (anode/cathode regions), as the probe went to a series of N tubs with small P-type regions in between.
- Below 4.5 µm depth, the probe reaches the P-type Si substrate, which has an average doping concentration of about 1.2×10^{15} cm^{-3}.

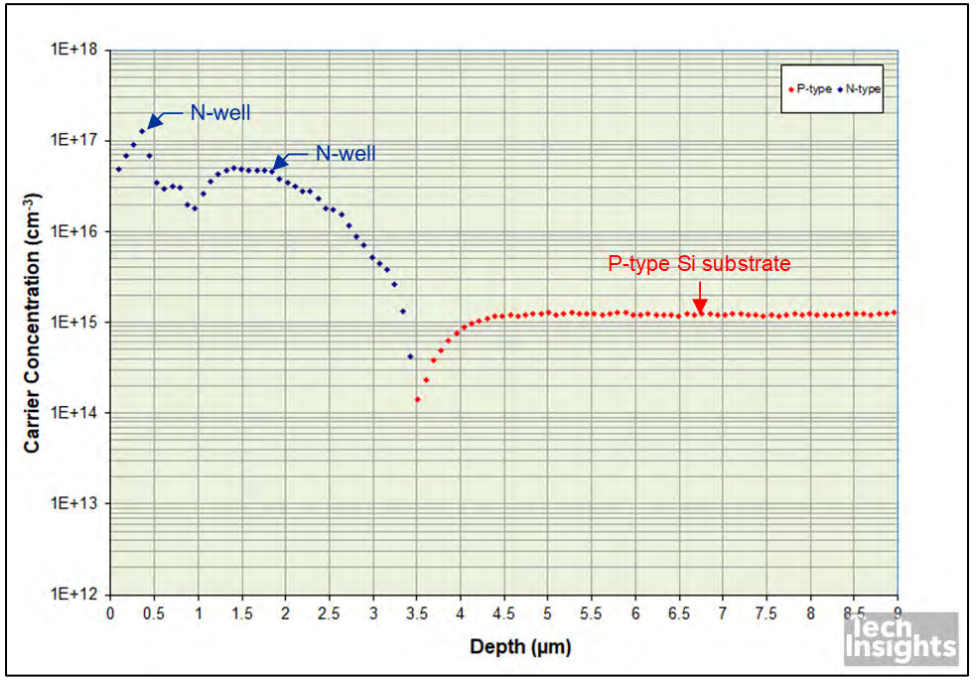


SRP_Profile_Pixel_Array.png

SPAD Array SRP Doping Profile

P- and N-Type Doping Profiles Logic – SRP

- SRP doping profile in the logic; probe load 5 Bevel Angle 0.02195 <100> Si X-step 4 µm.
- Near the surface, a first N-type doping concentration peak of 1.2 × 10^{17} cm^{-3}, likely corresponding to the contact region. Then at a depth of about 1.5 µm up to a depth of 3.5 µm, a second N-type doping concentration peak of 5 × 10^{16} cm^{-3}, which likely corresponds to the N-well. Below a depth of 3.5 µm it is the P-type Si substrate with a doping concentration of about 1.2 × 10^{15} cm^{-3}.

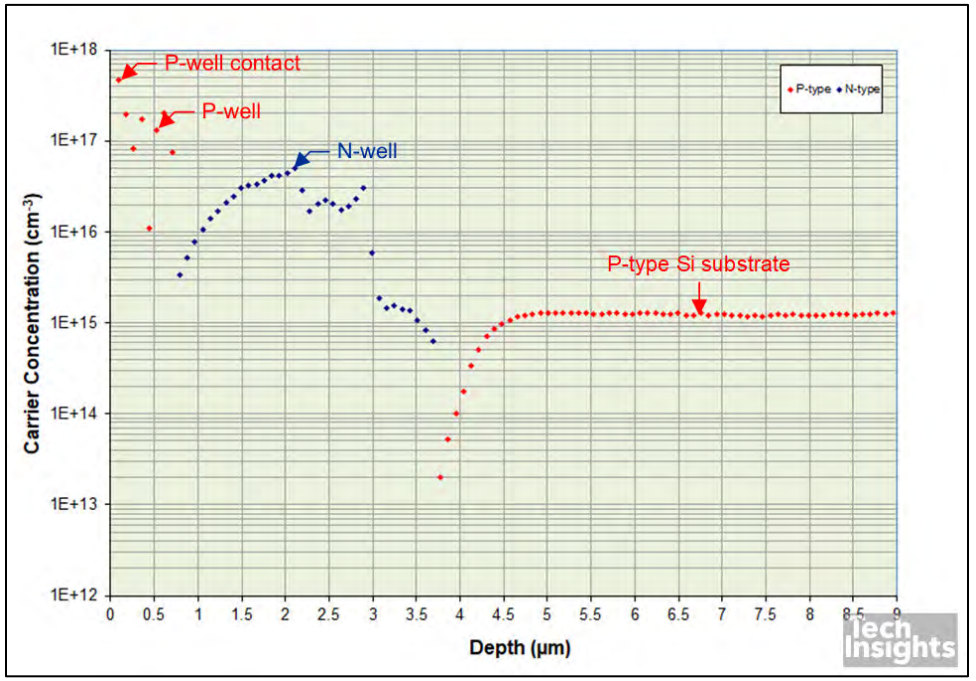


SRP_Profile_Logic.png

Logic SRP Doping Profile

P- and N-Type Doping Profiles Periphery – SRP

- SRP doping profile in the logic; probe load 2.6 Bevel Angle .02038 <100> Si X-step 4 µm.
- Near the surface, there is a P-type doped region with a doping concentration peak of 5 × 10^{17} cm^{-3}, which likely corresponds to a P-type contact region. Then at a depth of 0.5 µm, a P-type doping concentration of 1.2 × 10^{17} cm^{-3}, likely corresponds to a shallow P-well. Then at a depth of about 0.75 µm up to a depth of 3.75 µm there is a N-well, with a doping concentration peak of 5 × 10^{16} cm^{-3}. From a depth of 3.75 µm onward it is the P-type Si substrate with a doping concentration of about 1.2 × 10^{15} cm^{-3}.



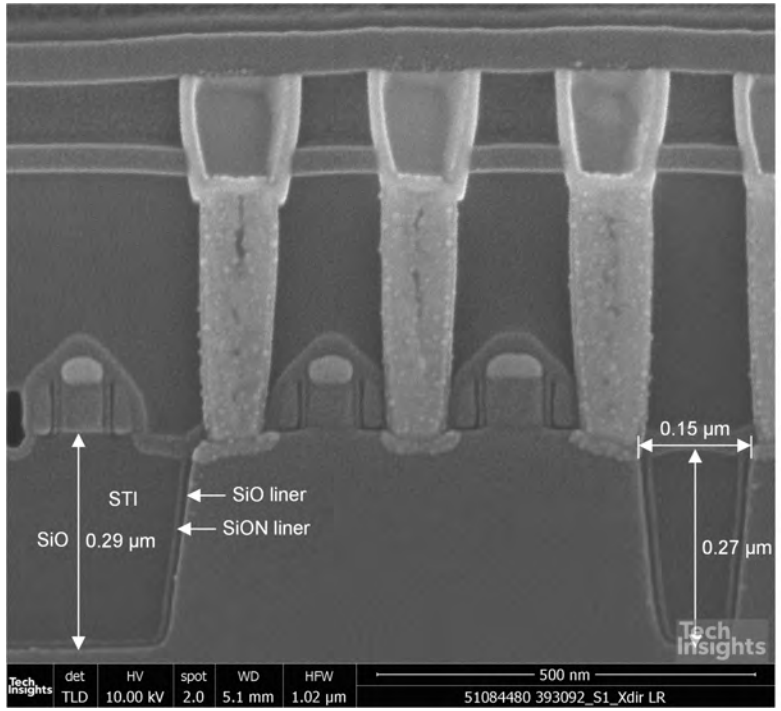
SRP_Profile_Periphery.png

Periphery SRP Doping Profile

Isolation Structures

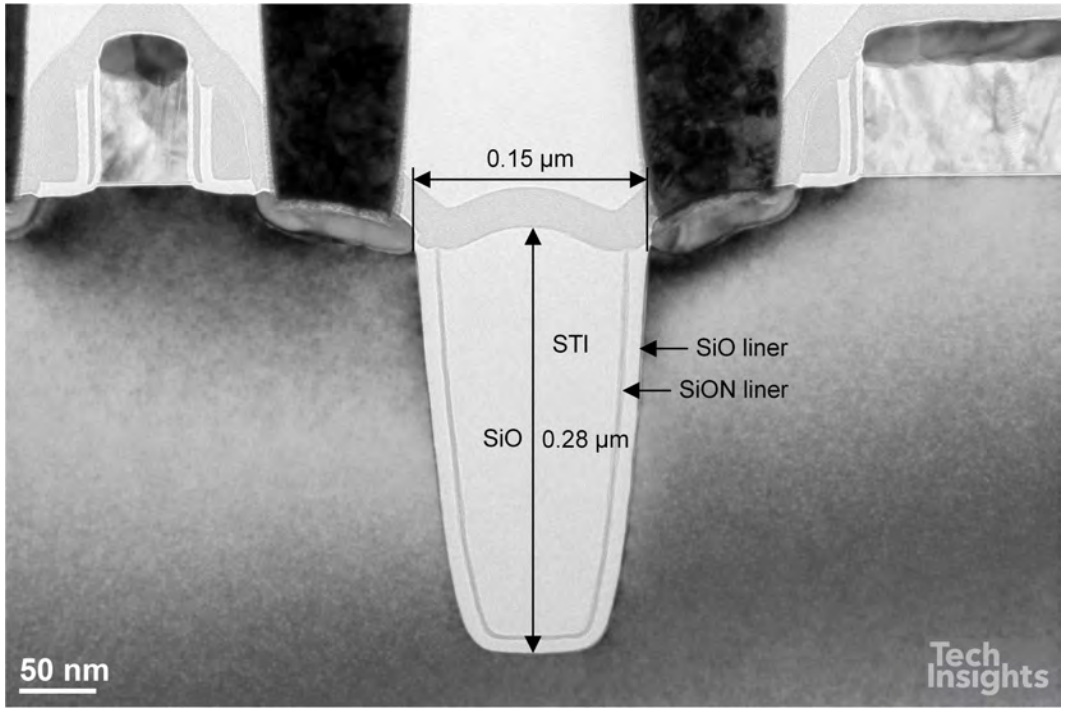
Isolation – STI

- SEM and TEM cross section images of the STI in the logic region. The STI in the logic and other regions of the die is the same.
- In the logic region the STI is 0.27-0.28 µm thick under the CESL nitride and 0.29 µm thick under the polysilicon.
- The STI is lined with oxide and SiON and filled with oxide.



588_Peripheral_MOS_393092.png

Logic Region STI – SEM

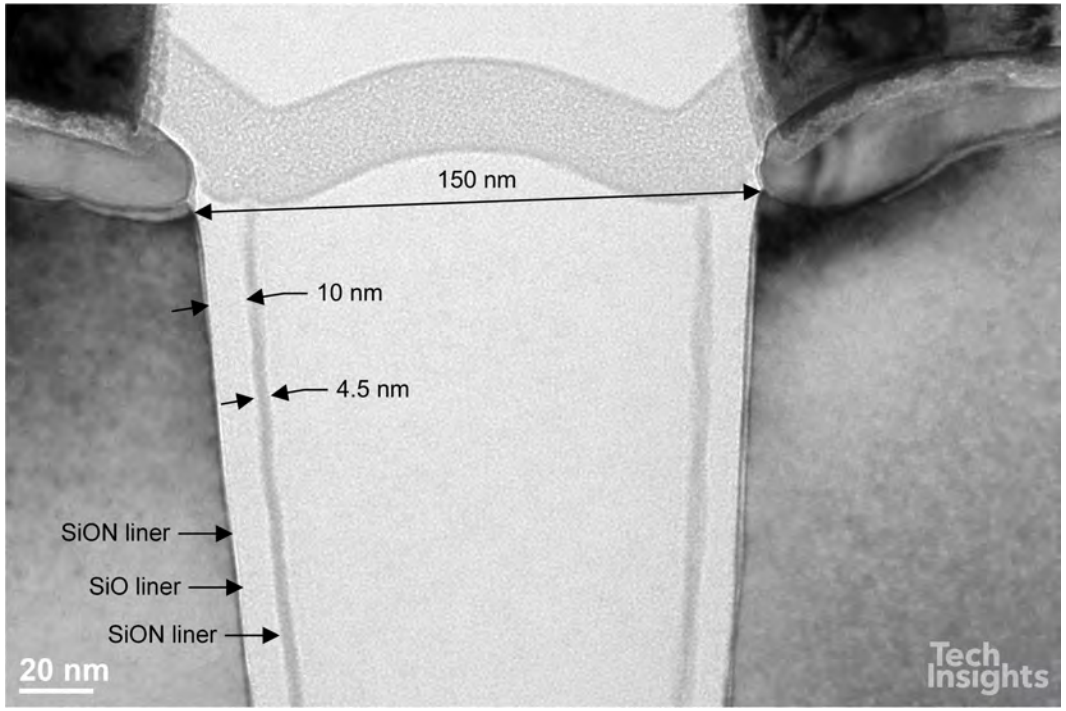


sti 35k_397216.png

Logic Region STI – TEM

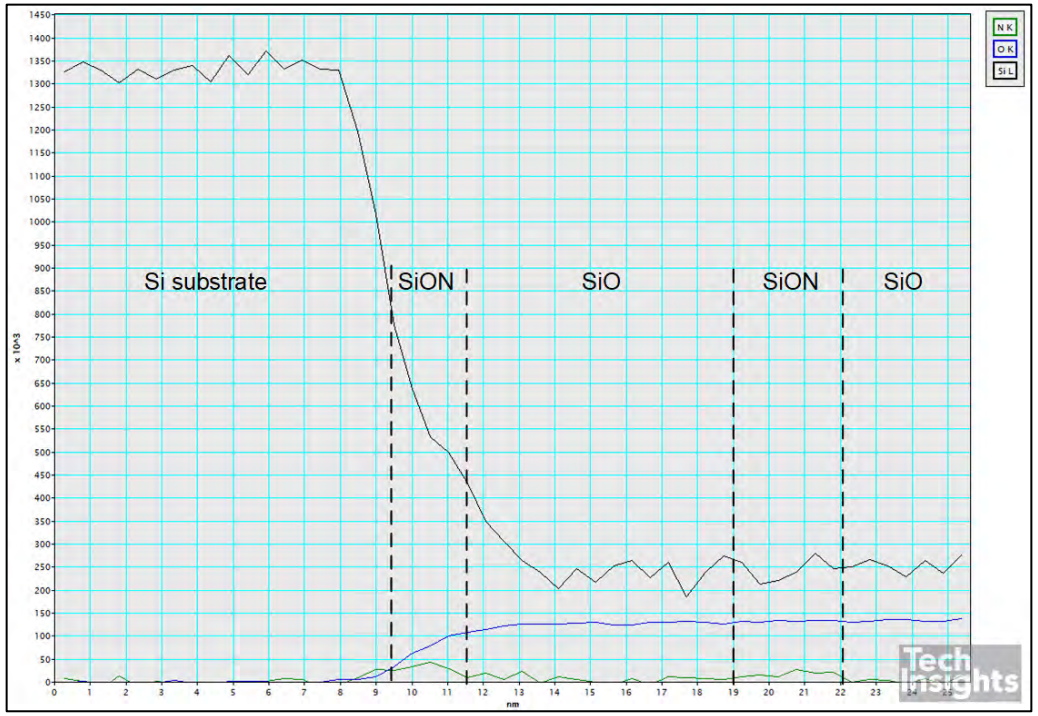
Isolation – STI

- TEM cross section detail and TEM-EELS image of the STI and STI liners
- The STI has a very thin SiON liner about 2 nm thick, then a 10 nm thick oxide liner and a 4.5 nm thick SiON liner.
- Note: Silicon was omitted from the TEM-EELS graphic, so that it was possible to observe the very weak nitrogen signal.



sti top 88k_397216.png

Logic Region STI Detail – SEM



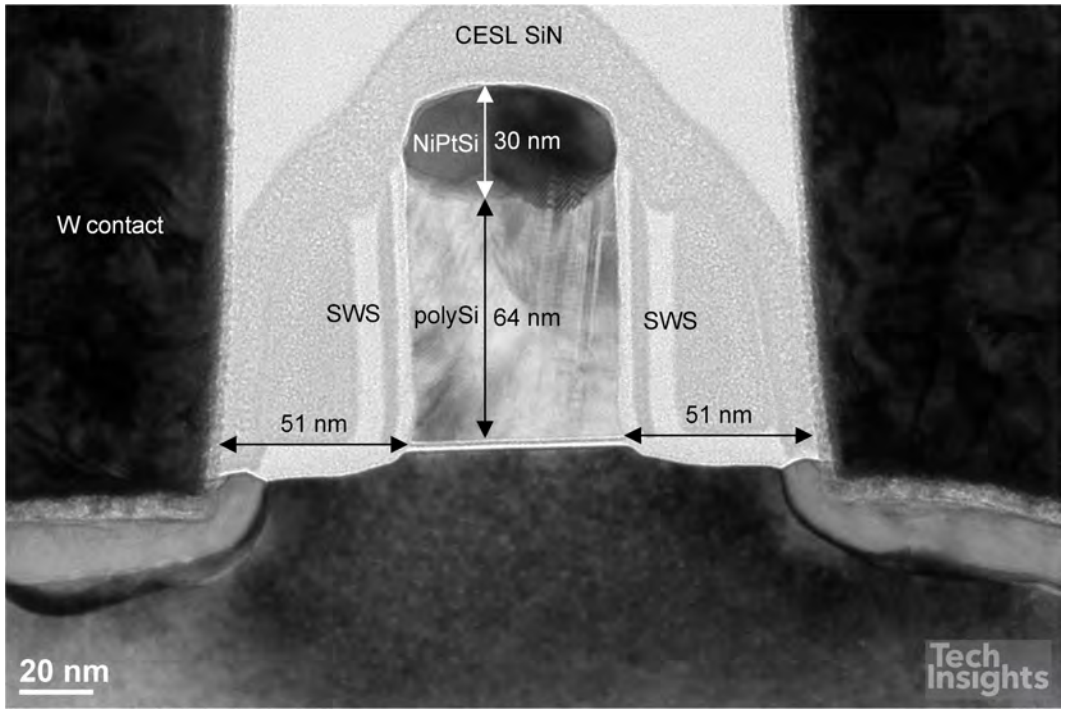
112225_EELS line scans__STI_397216.png

Logic Region STI – TEM-EELS

Poly and Pixel Transistors

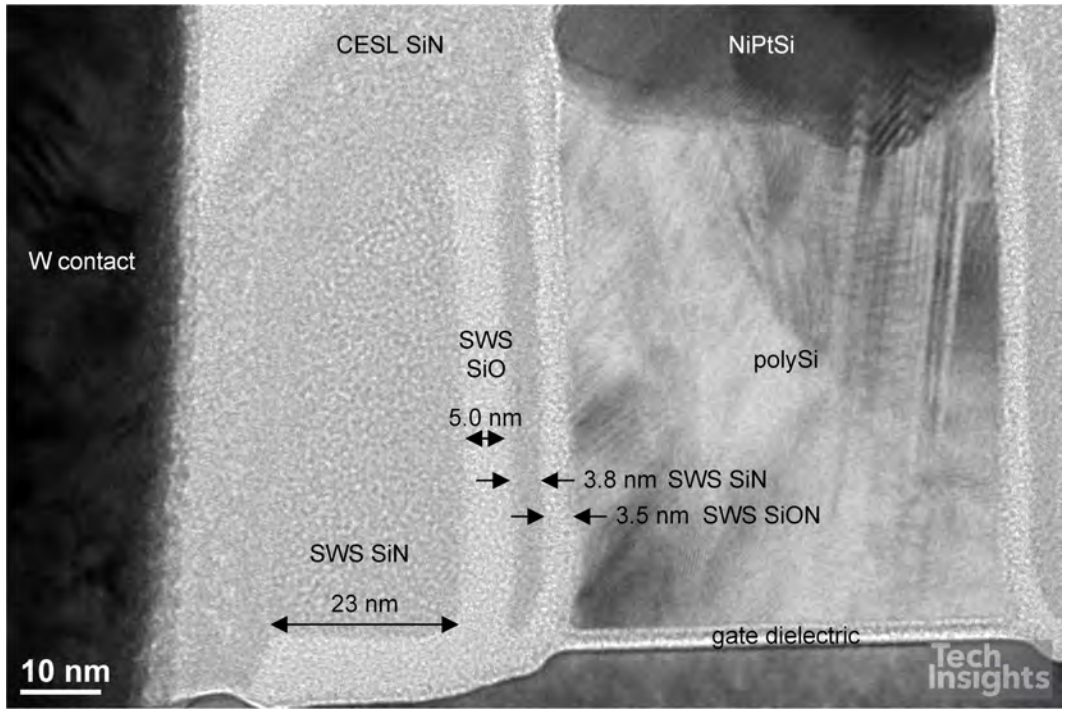
Transistors – Polysilicon Gates

- The logic and readout transistors have the same structure. They use one polysilicon gate layer with a total thickness of about 94 nm.
- The gate and S/D regions of I/O, logic and readout transistors use a NiPt silicide.
- The sidewall spacer (SWS) comprises a 3.5 nm thick I-shape SiON, a 3.8 nm thick I-shape SiN, a 5.0 nm thick L-shape oxide, and a 23 nm thick D-shape nitride. A CESL nitride covers the transistors.



logic gate_397216.png

Transistor Polysilicon Gate Overview – SEM



logic gate sws 180k_397216.png

Transistor SWS Detail – TEM

FEOL and BEOL Summary Tables

Front Dielectrics Summary

Layer	Composition (Based on TEM-EDS)	Thickness (nm)
Liner/pad oxide (silicide exclusion layer)	SiON/SiO	2/9
CESL	SiN	27
PMD	SiOP/SiOC/SiO/SiOC	240-280/33/8/78-90
ILD 1	SiCN/SiO/SiOC	53/30/280
ILD 2	SiCN/SiO/SiOC	55/30/300
ILD 3	SiCN/SiO/SiOC	55/30/300
ILD 4	SiCN/SiO/SiOC	50/30/270
ILD 5	SiCN/SiN[(b)]/SiO[(c)]/SiN[(c)]/SiO/SiN/SiO	44/31[(b)]/24[(c)]/46[(c)]/570/53/760
IMD 6	SiN/SiO/SiN/SiO	74/200/52/59
Passivation	SiO/SiN	270/95
Multilayer filter (36 layers)	Si/SiO	3.6 µm (total thickness)

(a) ILD 3, ILD 4 material composition inferred from similarity with ILD 1
(b) MIM capacitor dielectric
(c) MIM capacitor capping layer

Front Metals Summary

Layer	Composition (Based on TEM-EDS)	Thickness (nm)
Metal 1/liner	Cu/Ta-based	170/17
Metal 2/liner	Cu/Ta-based	240/17
Metal 3/liner	Cu/Ta-based	180/20
Metal 4/liner	Cu/Ta-based	210/14
MIM capacitor bottom electrode	Ta-based/Al/Ta-based	20/160/62
MIM capacitor top electrode	Ta-based	73
Metal 5/liner	Cu/Ta-based	160/21
Metal 6/liner	Cu/Ta-based	850/20
Metal 7/liner	TaN/Al/Ti-based	140/960/32

Transistor Summary

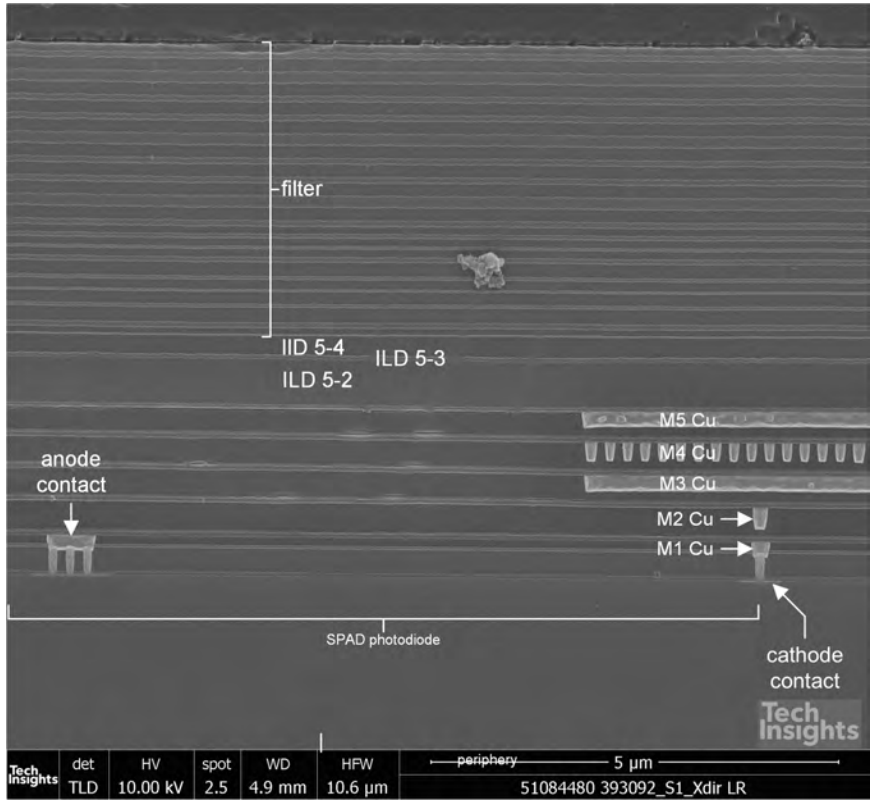
Transistor	Length (nm)	Gate Dielectric	Gate Dielectric Thickness (nm)
Logic	57	Nitrided oxide	2.8
SPAD readout circuitry	57	Nitrided oxide	2.8
SPAD readout circuitry	–	Nitrided oxide	3.7

Front Dielectrics and Metal Interconnect SPAD Array

Tech Insights

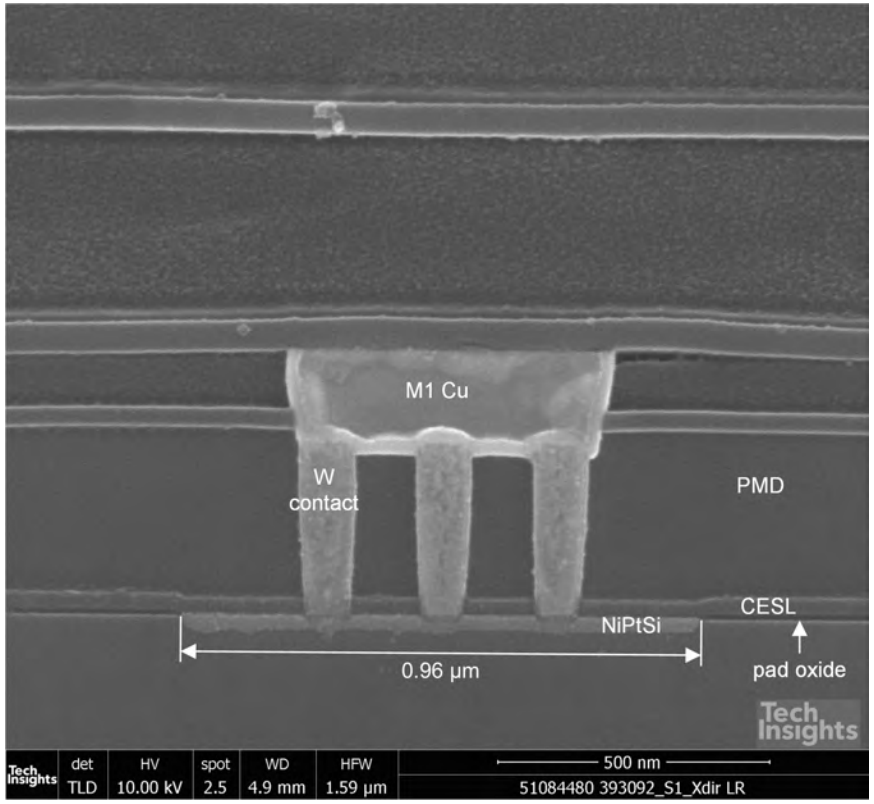
SPAD General Structure

- SEM cross section images showing half SPAD pixel and SPAD anode contact.
- There is a multilayer filter over the SPAD array region. The SPAD array uses five Cu interconnect layers.
- The anode has a 0.96 µm square NiPt silicided contact region. Outside of the silicided region there is a pad oxide layer between the CESL nitride and the Si.



904_Active_Array_Centre_of_SPAD_Pixel_393092.png

SPAD Pixel Overview – SEM

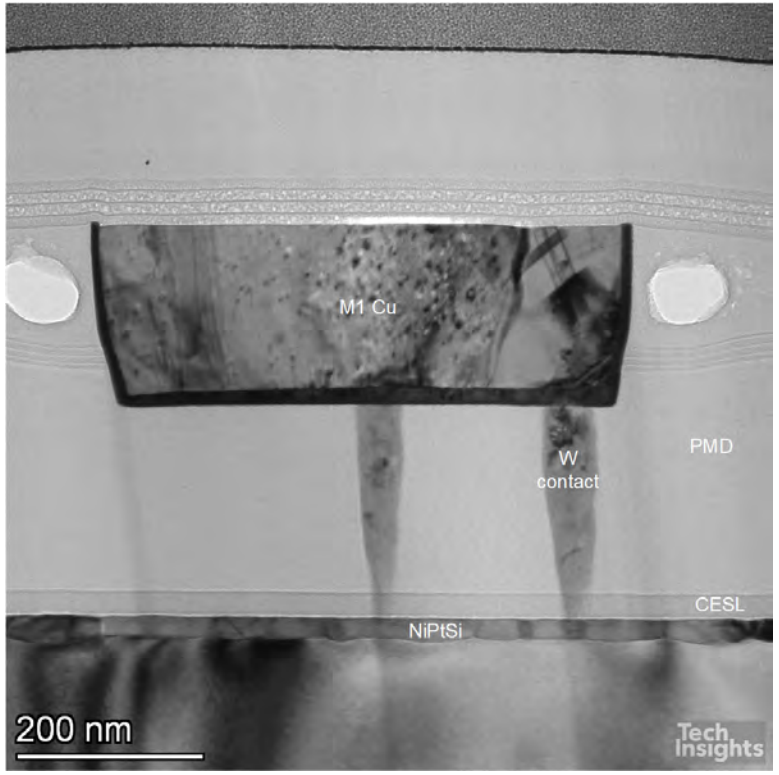


906_Active_Array_Centre_of_SPAD_Pixel_393092.png

SPAD Anode Contact – SEM

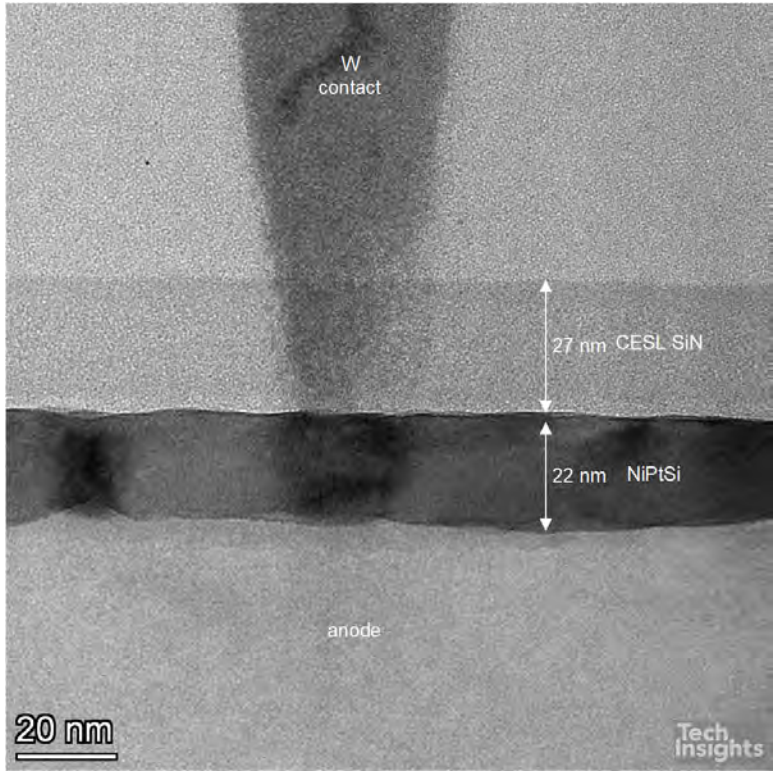
SPAD General Structure – Anode

- TEM cross section overview and detail images of the SPAD anode contacts.
- The anode has a 22 nm thick NiPt silicide, which is covered with the CESL nitride.



1358 36000 x Camera_400062.png

SPAD Anode Contacts Overview – TEM

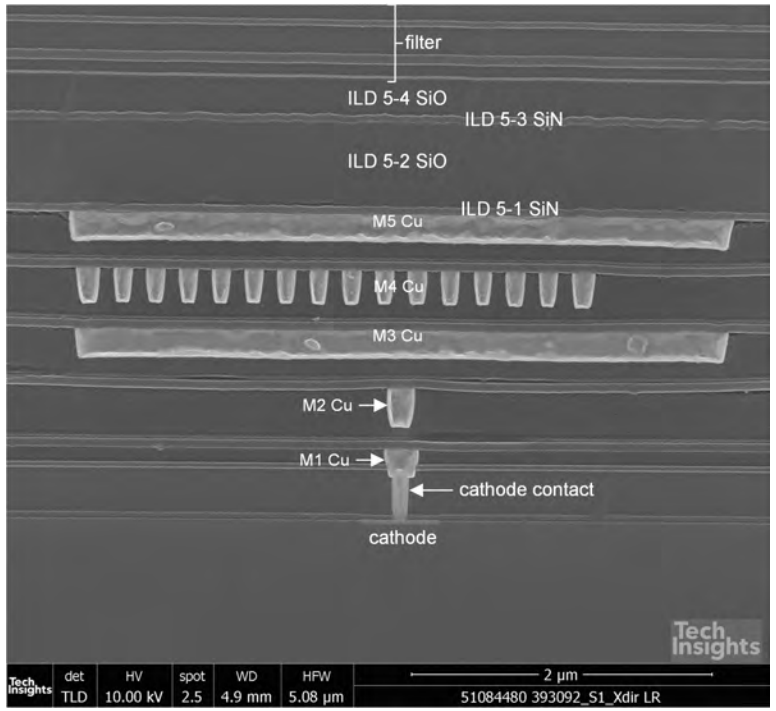


1403 190 kx Camera_400062.png

SPAD Anode Contact Detail – TEM

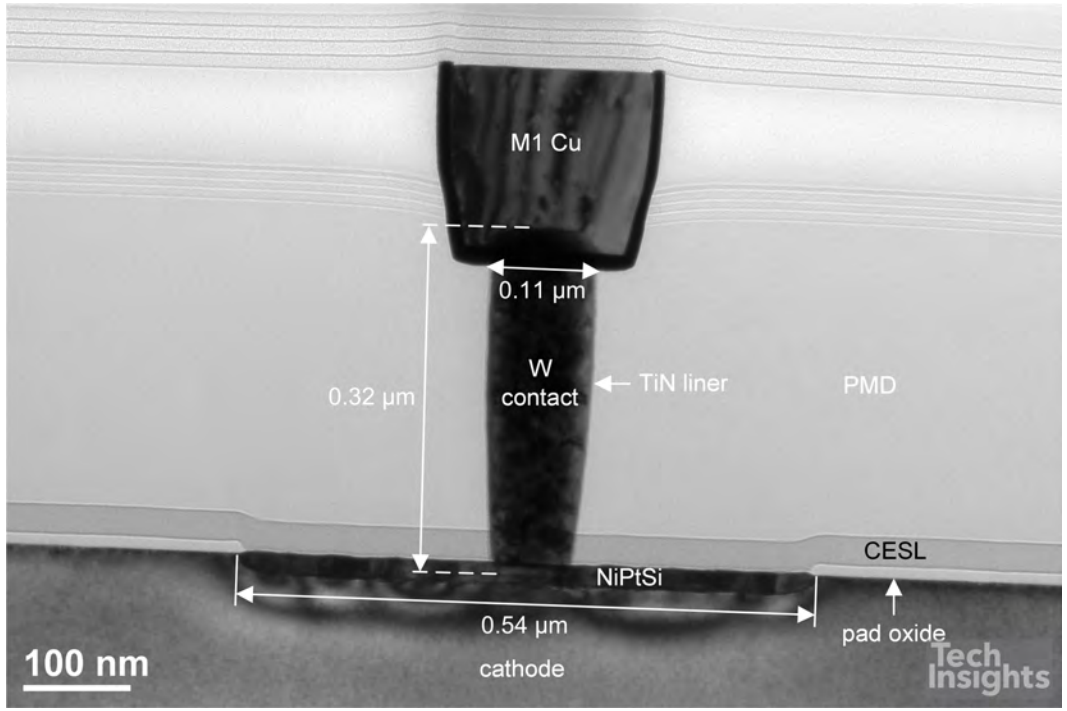
SPAD General Structure – Cathode

- SEM and TEM cross section images of the SPAD cathode contact region.
- The cathode has a 0.54 µm wide NiPt silicide region.
- The W contact is 0.32 µm thick, 0.11 µm wide at the top, and has a TiN liner.
- Outside of the silicided region there is a pad oxide layer between the CESL nitride and the Si.



907_Active_Array_Centre_of_SPAD_Pixel_393092.png

SPAD Cathode Contact Overview – SEM

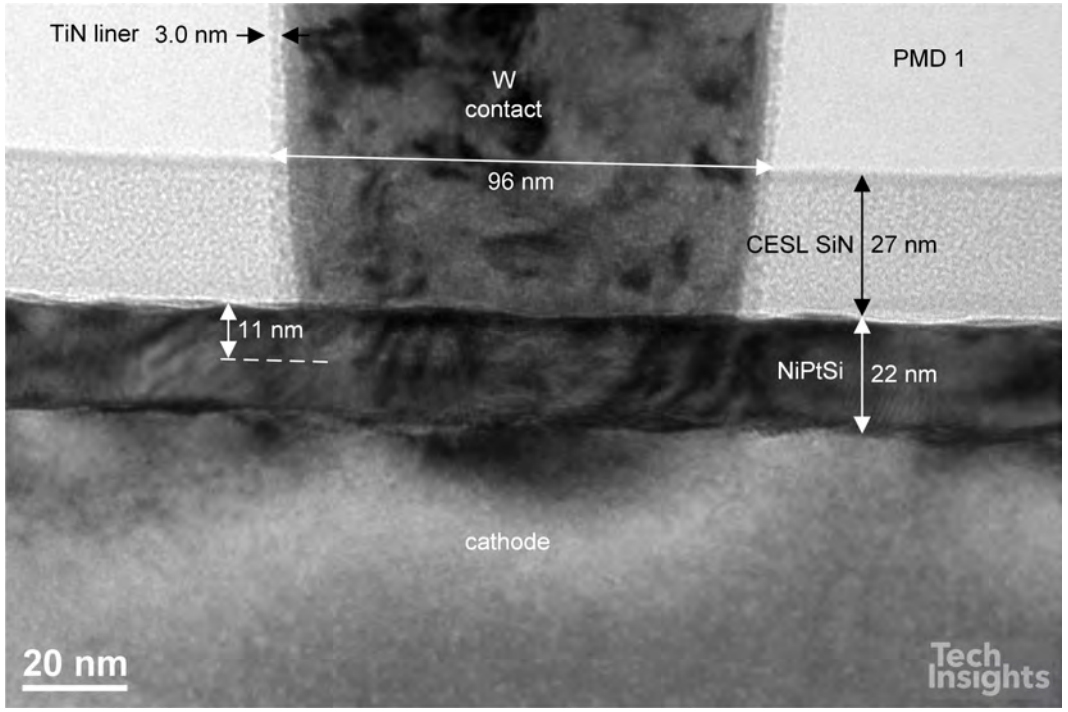


spad- pmd 27k_397216.png

SPAD Cathode Contact Detail – TEM

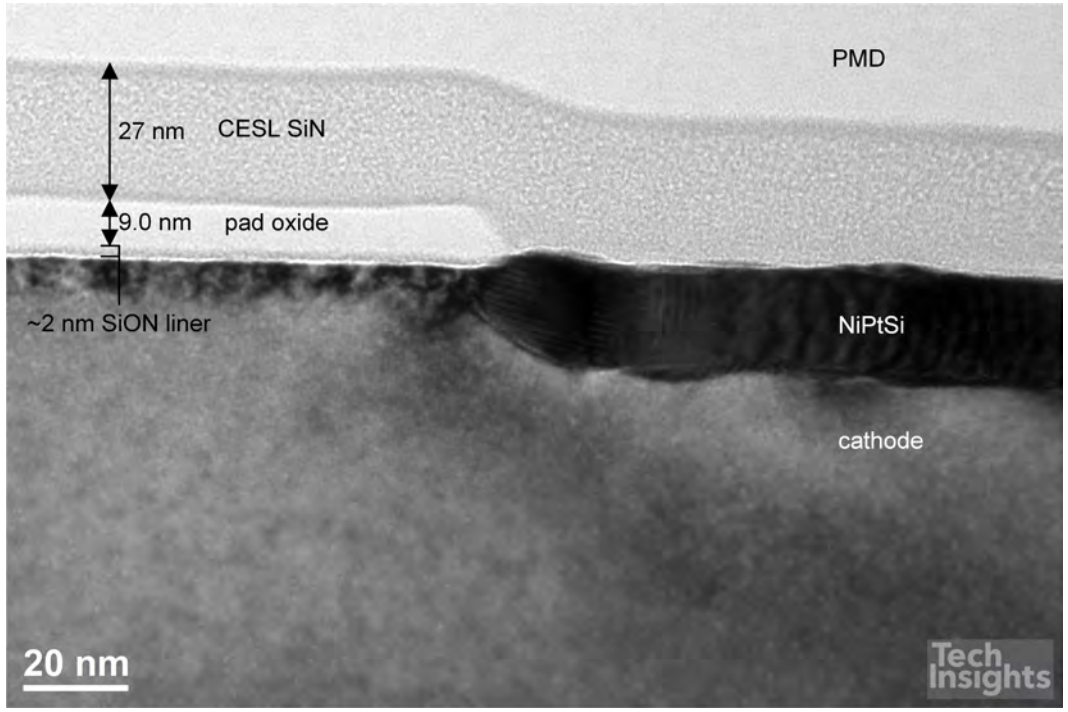
SPAD General Structure Cathode

- TEM cross section images of the SPAD cathode contact region.
- The cathode contact is 96 nm wide at the bottom, and the TiN liner is 3 nm thick. The W contact penetrates about 11 nm into the NiPt silicide.
- NiPt silicide region is 22 nm thick and is covered with a 27 nm thick CESL nitride.
- Outside of the cathode silicide region there is an ~2 nm thick SiON liner and a 9 nm thick pad oxide layer (silicide blocking layer).



spad-cont to subtrate 130k_397216.png

SPAD Cathode Contact Bottom Detail – TEM

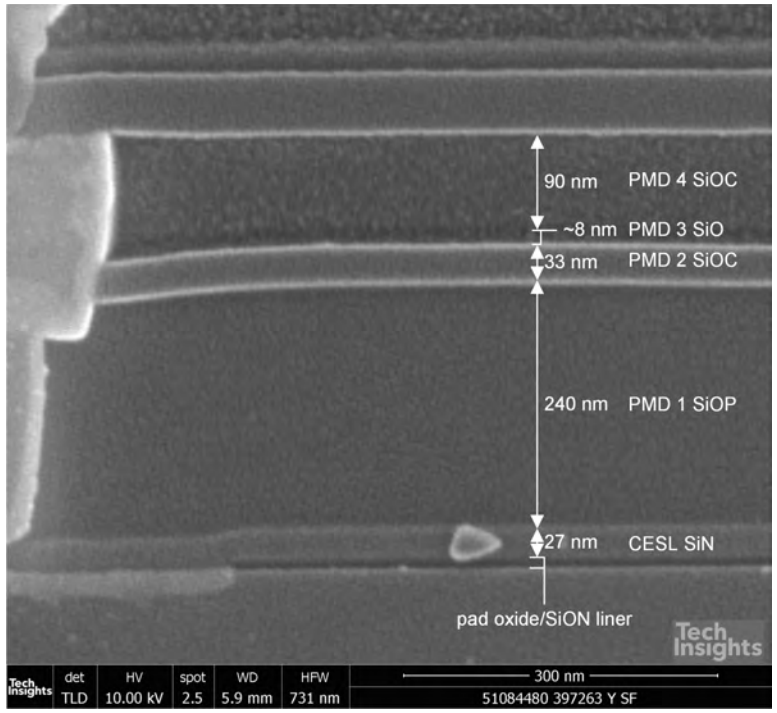


spad- subtrate -silicide edge 130k_397216.png

SPAD Cathode Contact Silicide Edge Detail – TEM

SPAD Front Dielectrics and Metals

- The SPAD pixel, readout circuitry, logic, and I/O regions use the same PMD layers.
- In the SPAD region, the PMD comprises 2 nm thick SiON liner and a 9 nm thick pad oxide (see next page), a 27 nm thick CESL nitride, a 240-280 nm thick PMD 1 SiOP (two samples with different thicknesses), a 33 nm thick PMD 2 SiOC, an 8 nm thick PMD 3 oxide, and a 78-90 nm thick PMD 4 SiOC.



024_array_SPAD_PMD_397263.png

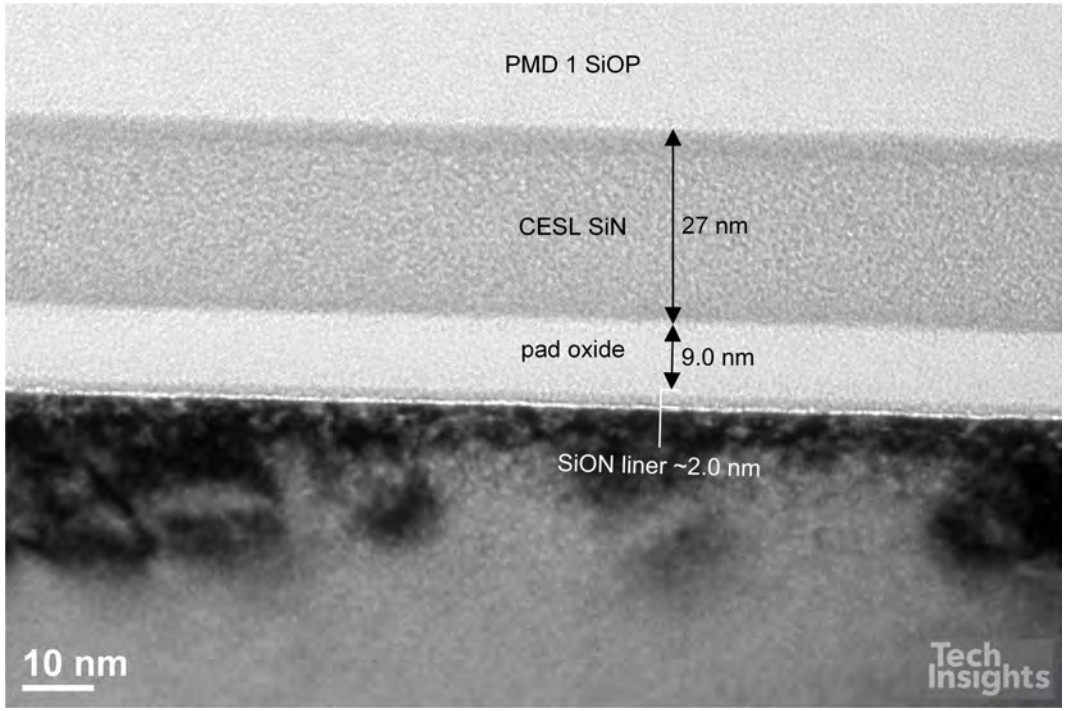
SPAD PMD – SEM

spad-pmd 35k_397216.png

SPAD PMD – TEM

SPAD Front Dielectrics and Metals

- The SPAD lower layers comprise an approximately 2 nm thick SiON liner and a 9 nm thick pad oxide and a 27 nm thick CESL nitride.

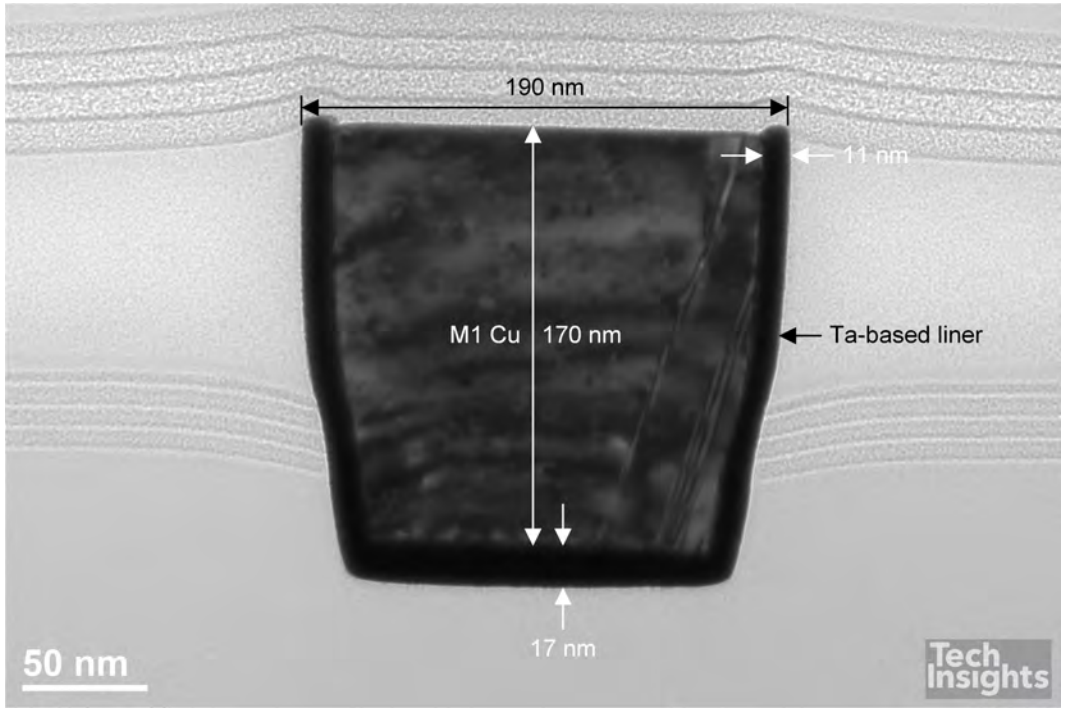


spad_pmd lower layer over si subts 180k_397216.png

SPAD PMD Lower Layers – TEM

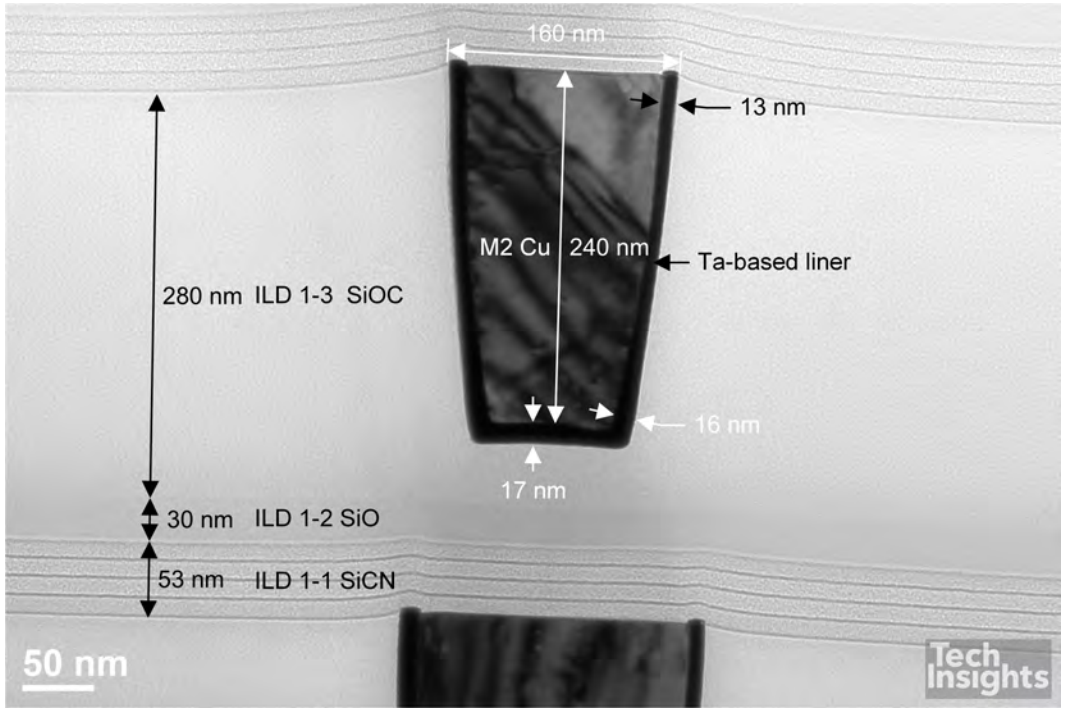
SPAD Front Dielectrics and Metals

- Metal 1 is a 170 nm thick Cu single damascene with a 17 nm thick Ta-based liner.
- Metal 2 is a 240 nm thick dual damascene Cu with a 17 nm thick Ta-based liner
- ILD 1 comprises a 53 nm thick ILD 1-1 SiCN, a 30 nm thick ILD 1-2 oxide, and a 280 nm thick ILD 1-3 SiOC.



spad-m1 64k b_397216.png

Metal 1 – TEM

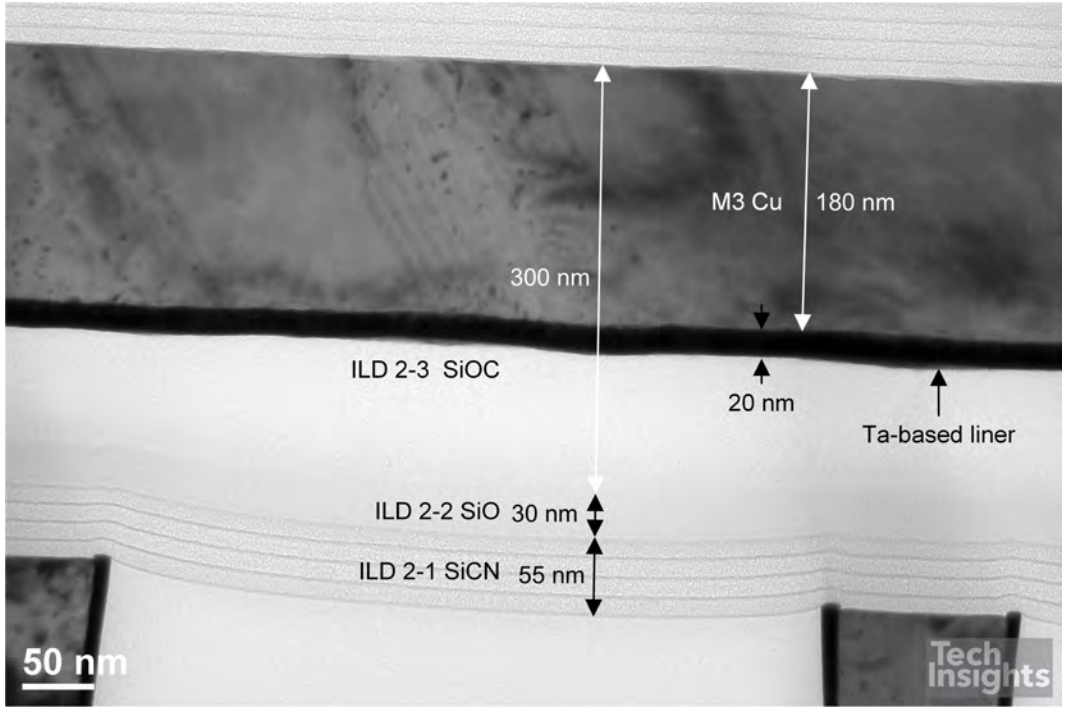


spad-ild 1 m2 35k_397216.png

ILD 1 and Metal 2 – TEM

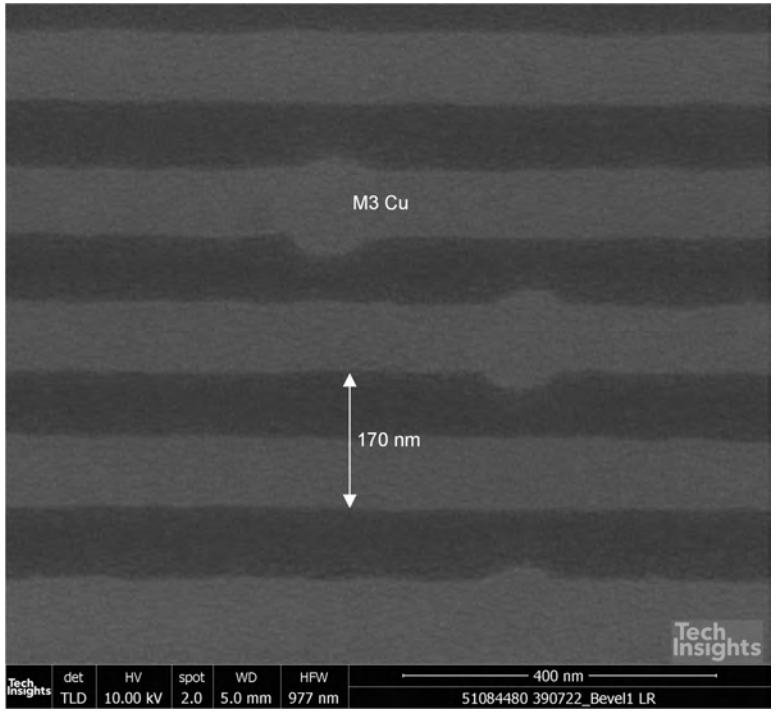
SPAD Front Dielectrics and Metals

- ILD 2 comprises a 55 nm thick ILD 2-1 SiCN, a 30 nm thick ILD 2-2 oxide, and a 300 nm thick ILD 2-3 SiOC.
- Metal 3 is 180 nm thick Cu with a 20 nm thick Ta-based liner.
- The minimum metal pitch of 170 nm was observed on metal 3.



spad-ild 2 to m3 35k_397216.png

ILD 2 and Metal 3 – TEM

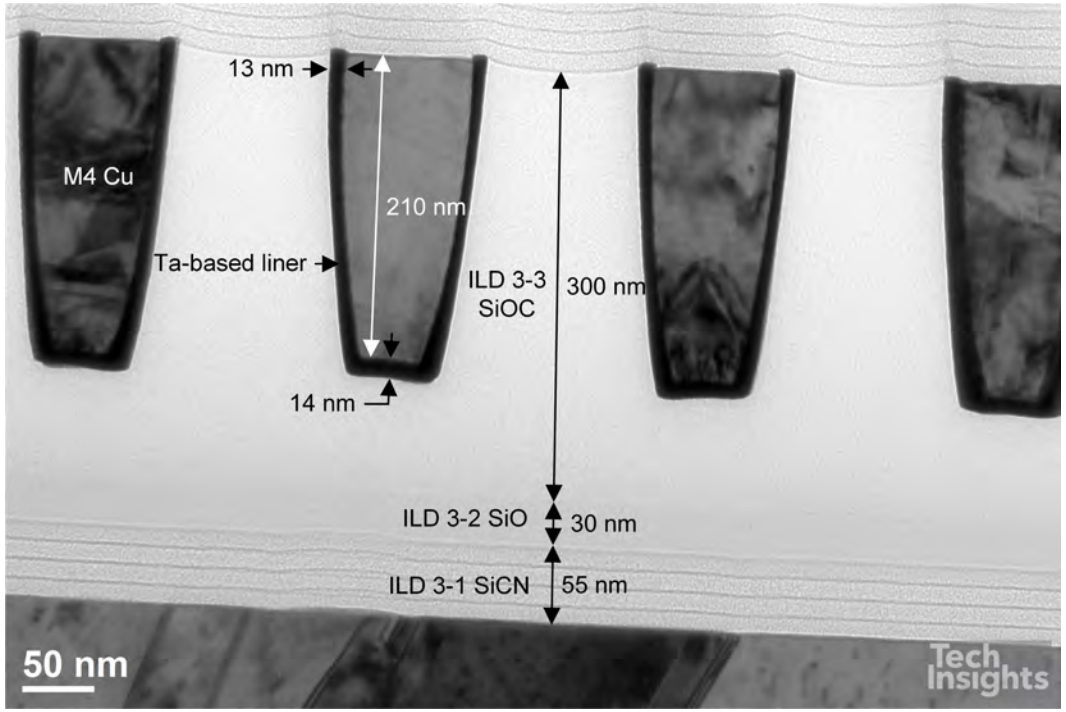


314_Bevel1_Array_M3_165nm_Pitch_390722.png

Metal 3 Minimum Pitch – SEM Plan-View

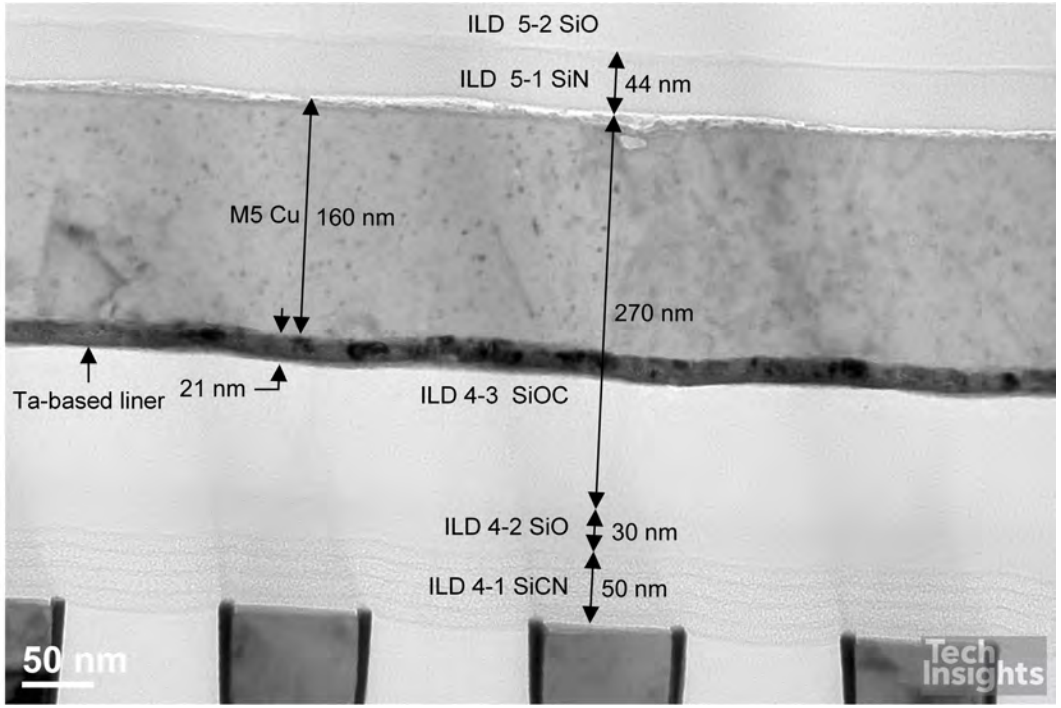
SPAD Front Dielectrics and Metals

- ILD 3 comprises a 55 nm thick ILD 3-1 SiCN, a 30 nm thick ILD 3-2 oxide, and a 300 nm thick ILD 3-3 SiOC.
- Metal 4 is 210 nm thick Cu with a 14 nm thick Ta-based liner.
- ILD 4 comprises a 50 nm thick ILD 4-1 SiCN, a 30 nm thick ILD 4-2 oxide, and a 270 nm thick ILD 4-3 SiOC.
- Metal 5 is 160 nm thick Cu with a 21 nm thick Ta-based liner.
- ILD 5-1 is a 44 nm thick nitride.



spad- ild 3_m4 35k_397216.png

ILD 3 and Metal 4 – TEM

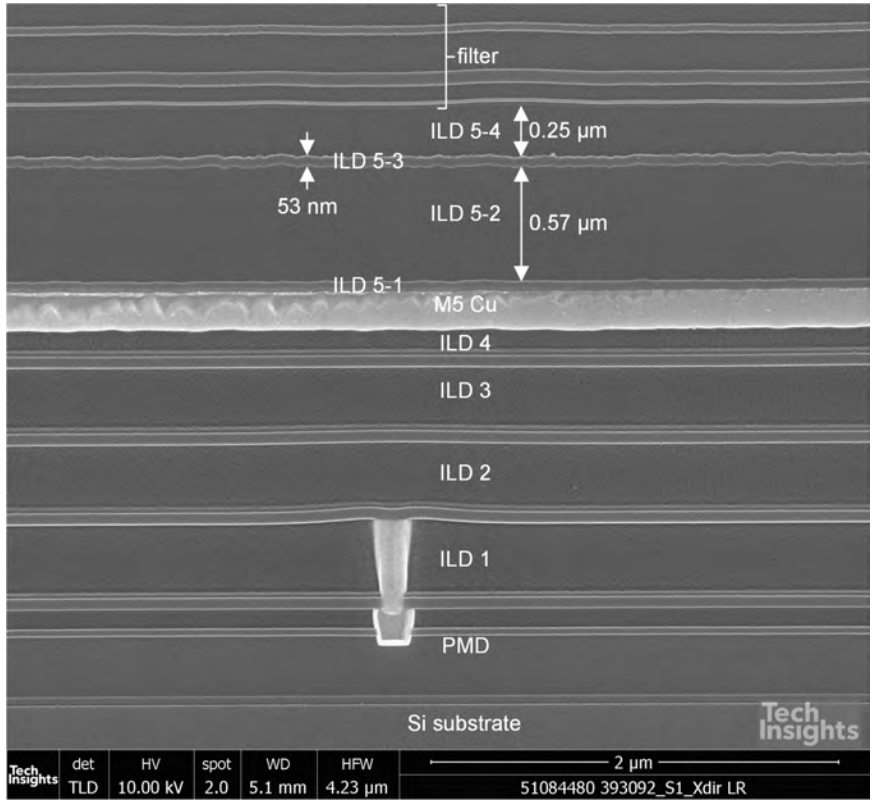


spad_ild4 and m5 35k_397216.png

ILD 4 and Metal 5 – TEM

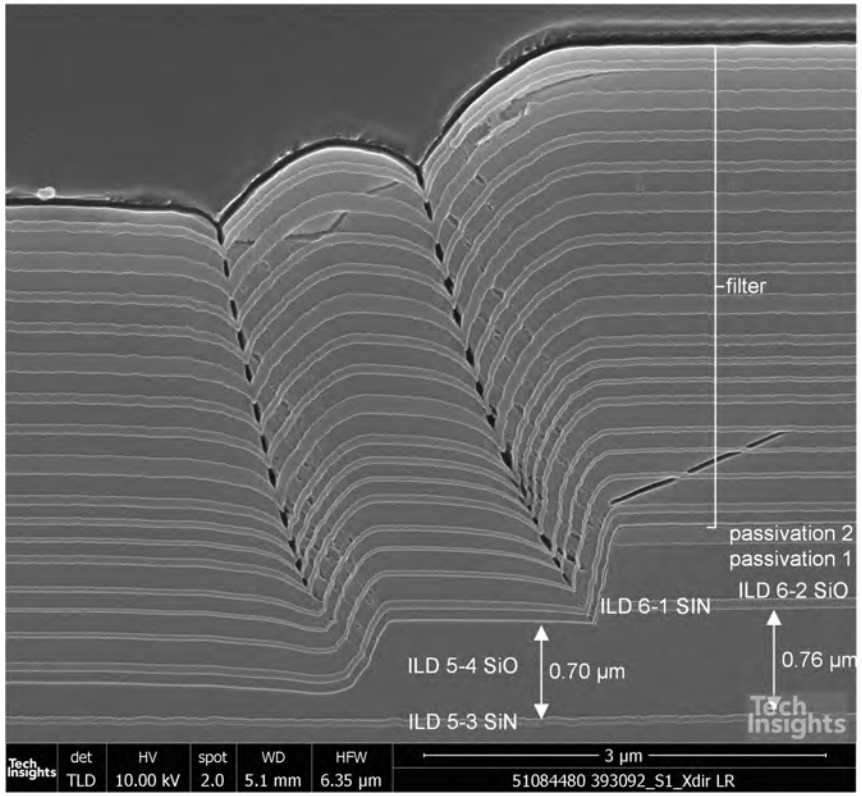
SPAD Front Dielectrics and Metals

- Over the SPAD array, the passivation, IMD 6, and a portion of ILD 5-4 layers are etched.
- ILD 5 comprises a 44 nm thick ILD 5-1 nitride, a 0.57 µm thick ILD 5-2 oxide, a 53 nm thick ILD 5-3 nitride, and a thinned 0.57 µm thick ILD 5-4 oxide.
- At the edge of the active SPAD array, there is a step in ILD 5-4; at this location, the full thickness of ILD 5-4 is 0.76 µm thick.



531_Pixel4_Active_SPAD_Array_Slice_B_393092.png

ILD 5 – SEM

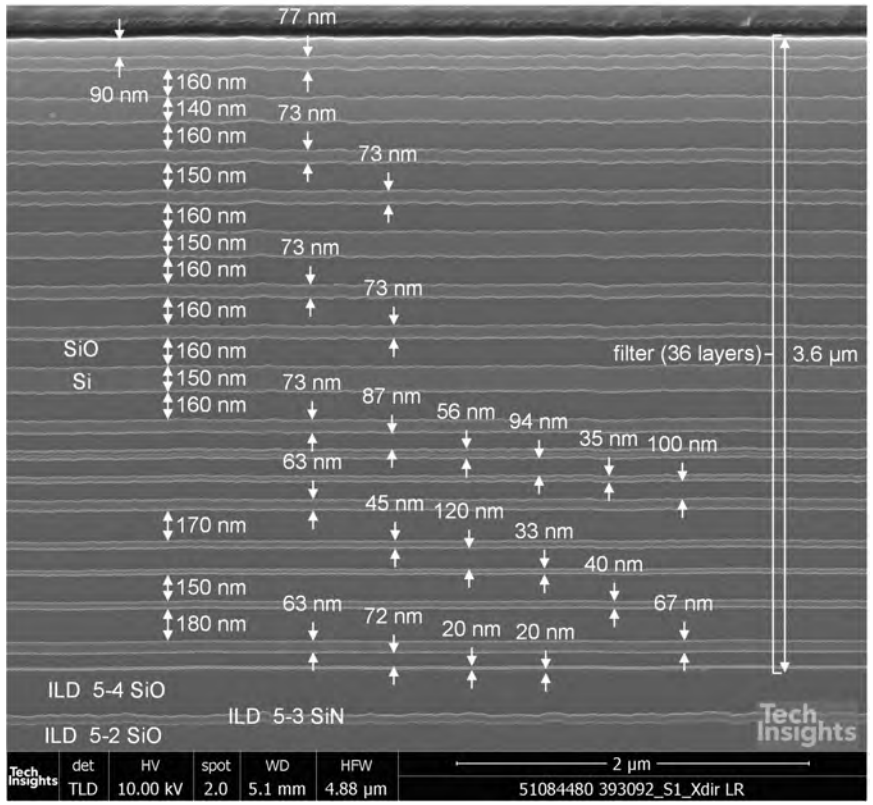


517_Active_SPAD_Array_Coating_393092.png

ILD 5-4 – SEM

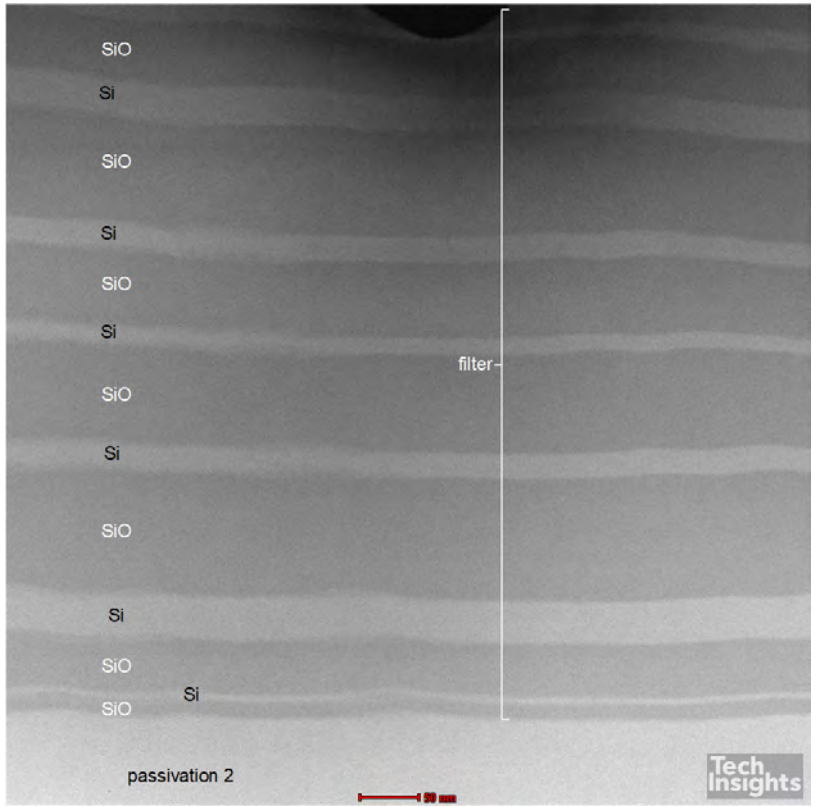
SPAD Front Dielectrics and Metals

- A multilayer filter is formed over the active SPAD, shielded SPAD, and some other regions of the die.
- The multilayer filter comprises 36 layers of oxide and amorphous silicon with different thicknesses, and a total thickness of 3.6 µm.



520_Active_SPAD_Array_Coating_393092.png

Multilayer Filter – SEM



100755_bottom part_Acquire HAADF_399357.png

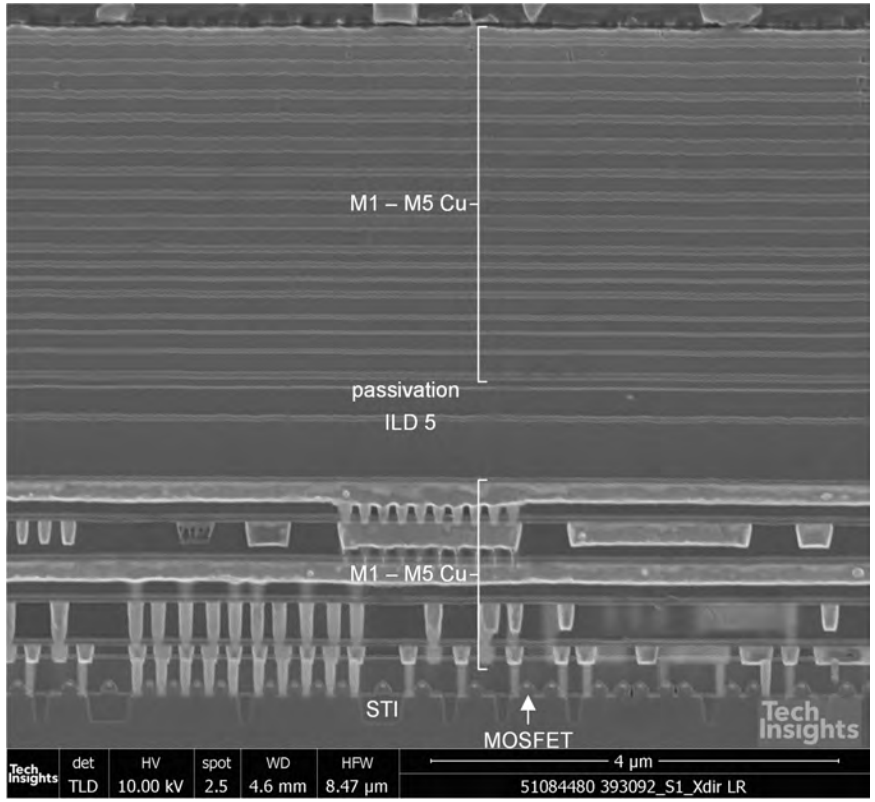
Multilayer Filter Detail – STEM

SPAD Array Readout Circuit Transistors

Tech Insights

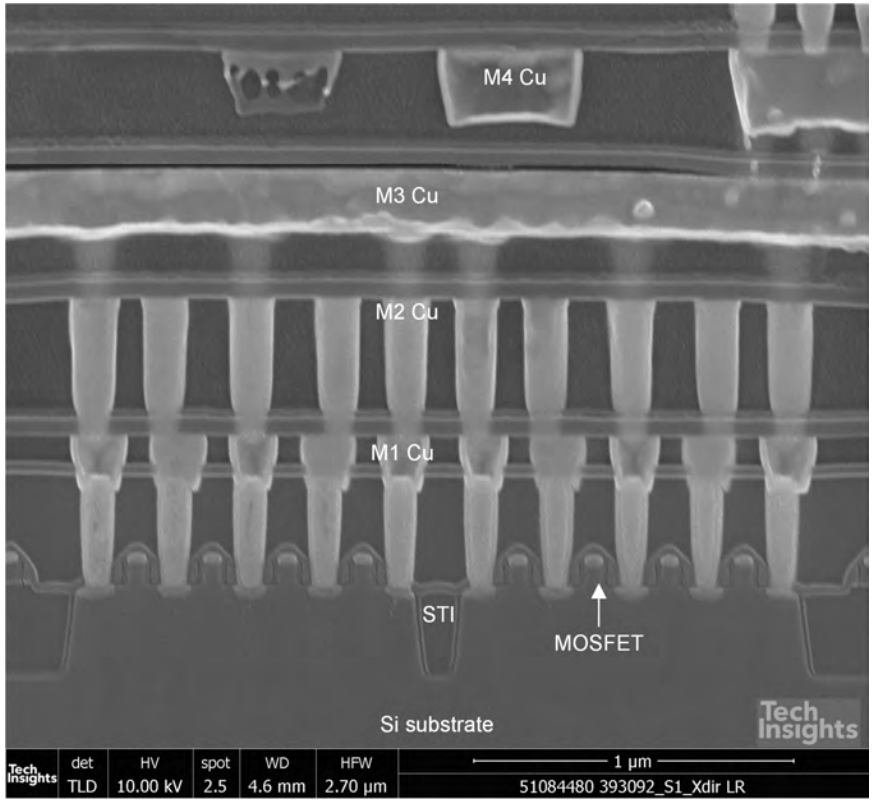
SPAD Array Readout Circuitry Transistors

- SEM cross section images showing the general structure in the SPAD array readout circuitry region.



854_Active_SPAD_393092.png

Readout Circuitry Transistors Overview – SEM

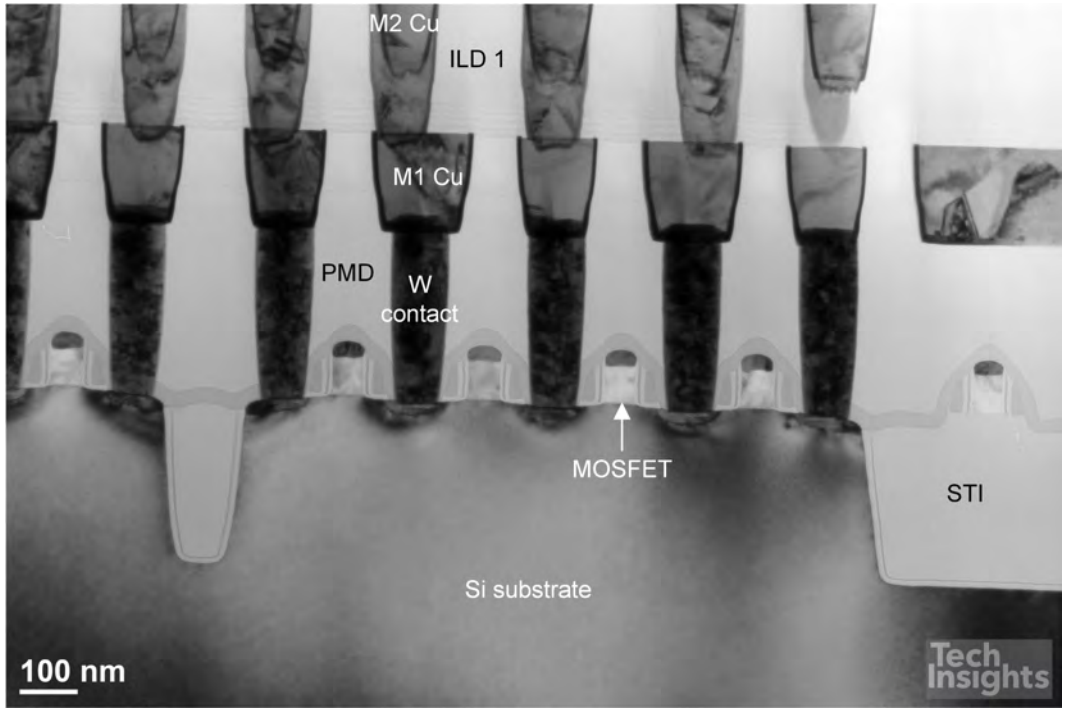


855_Active_SPAD_393092.png

Readout Circuitry Transistors Detail – SEM

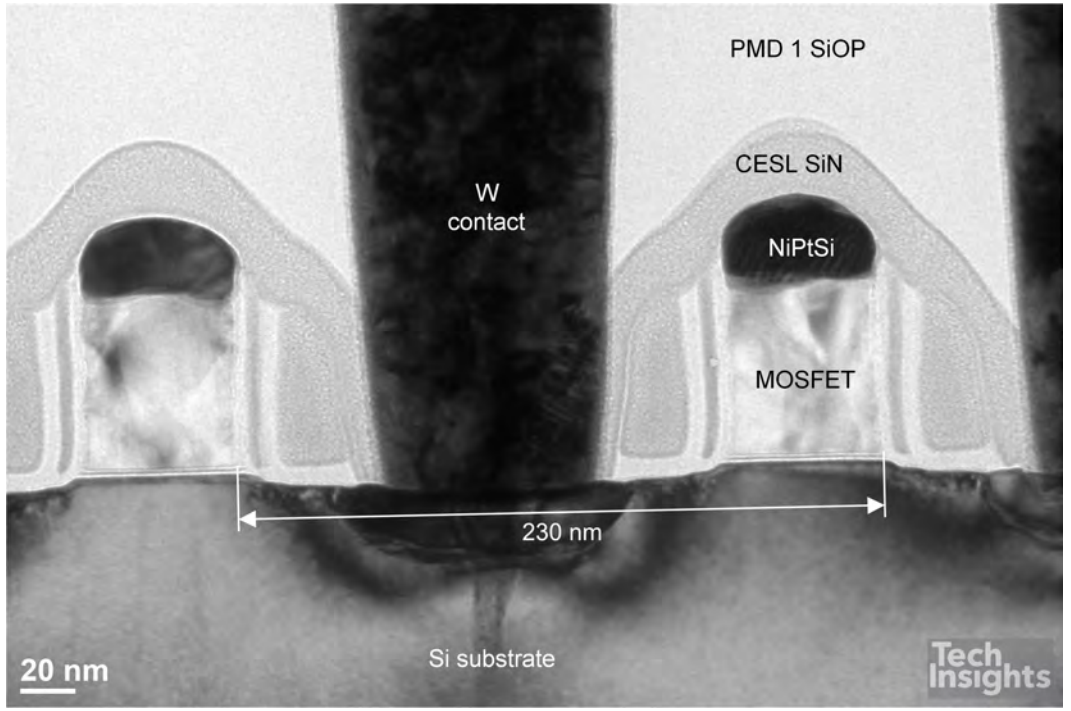
SPAD Array Readout Circuitry Transistors

- TEM cross section overview and detail images of the minimum size readout transistors.
- The minimum contacted gate pitch observed in the readout circuitry transistor is 230 nm, which is in line with the 65 nm process node.



readout 14k_e_399150.png

Readout Circuitry Transistors Overview – TEM

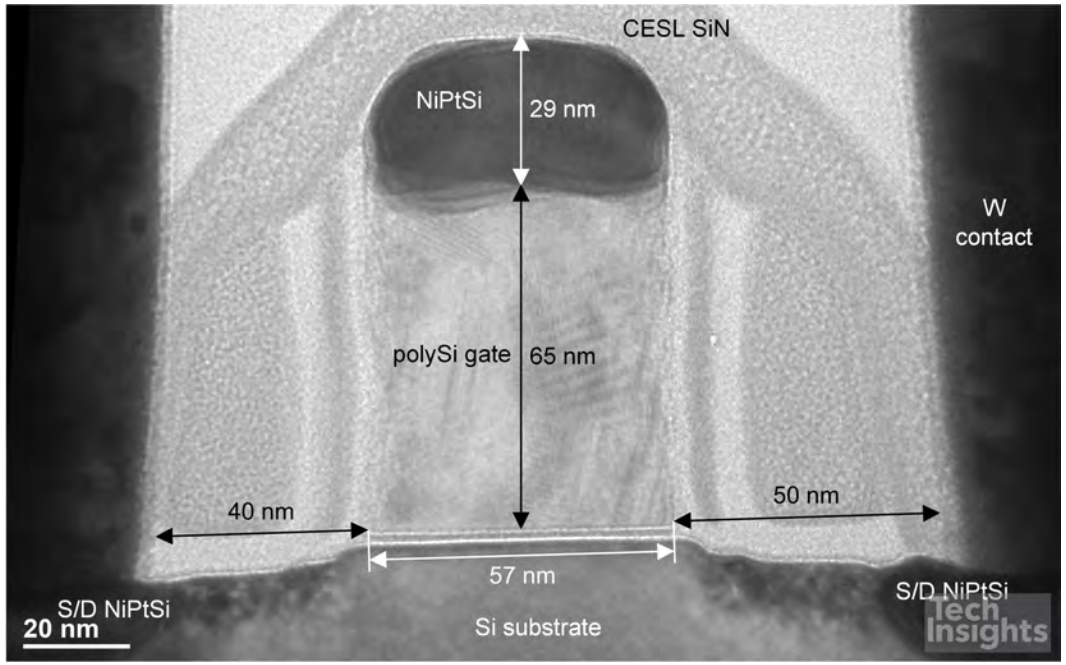


readout 64k g_399150.png

Readout Circuitry Transistors Detail – TEM

SPAD Array Readout Circuitry Transistors

- The length of the minimum size readout circuitry transistors is 57 nm, which is the same as the logic transistor.
- The polysilicon gate and S/D regions are NiPt silicided.

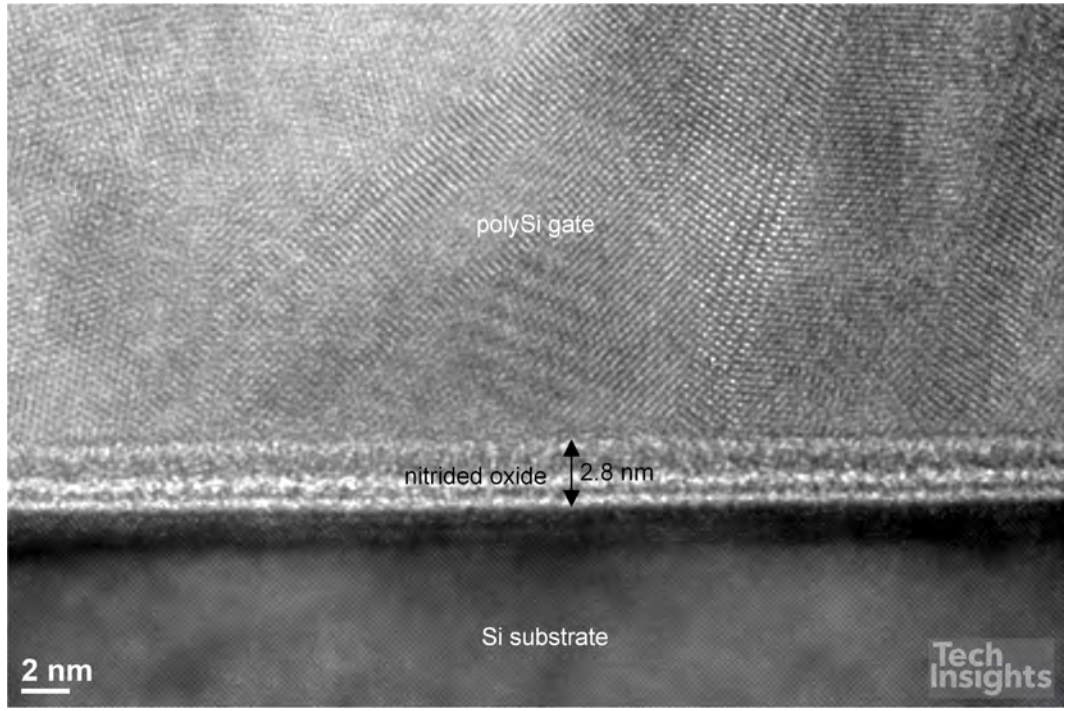


readout 130k e_rc_399150.png

Readout Circuitry Transistor Close-Up – TEM

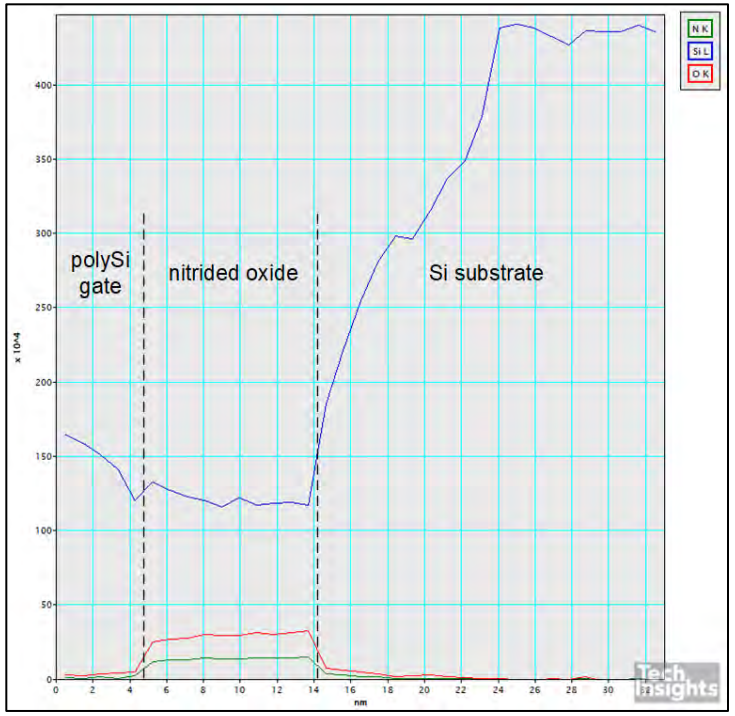
SPAD Array Readout Circuitry Transistors

- TEM and TEM-EELS images showing the gate dielectric of the readout circuitry transistor.
- The logic transistor gate dielectric is 2.8 nm thick nitrided oxide.



s gate_readout_go 530k g2_399150.png

Readout Circuitry Transistor Gate Dielectric – TEM

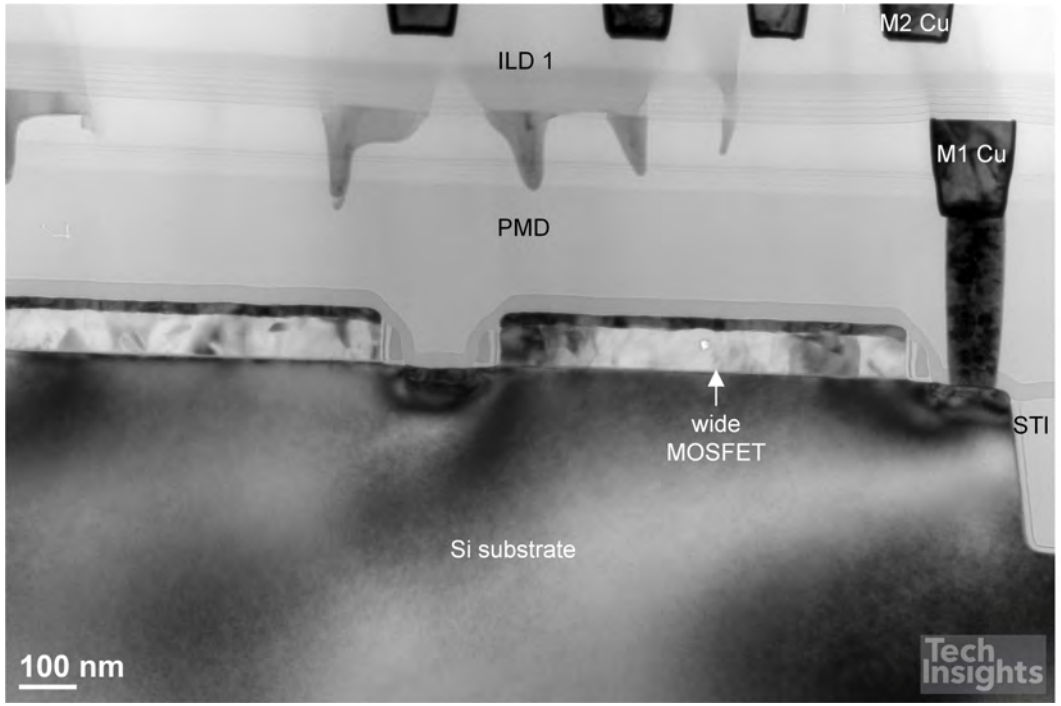


114519_EELS line scan_small gate dielectric_399150.png

Readout Circuitry Transistor Gate Dielectric – TEM-EELS

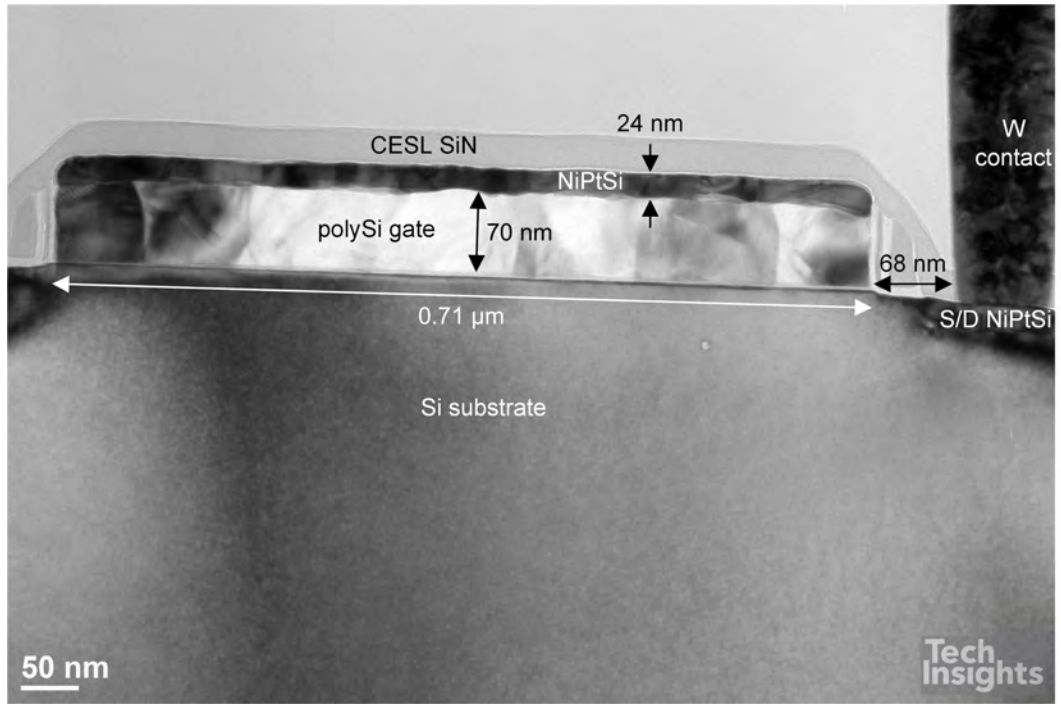
SPAD Array Readout Circuitry Transistors

- TEM cross section overview and detail images of the longer readout transistors.
- Different lengths of longer size transistors are used in the SPAD readout circuitry (see page 117).



readout_large gates 14k_399150.png

Readout Circuitry Longer Transistors Overview – TEM

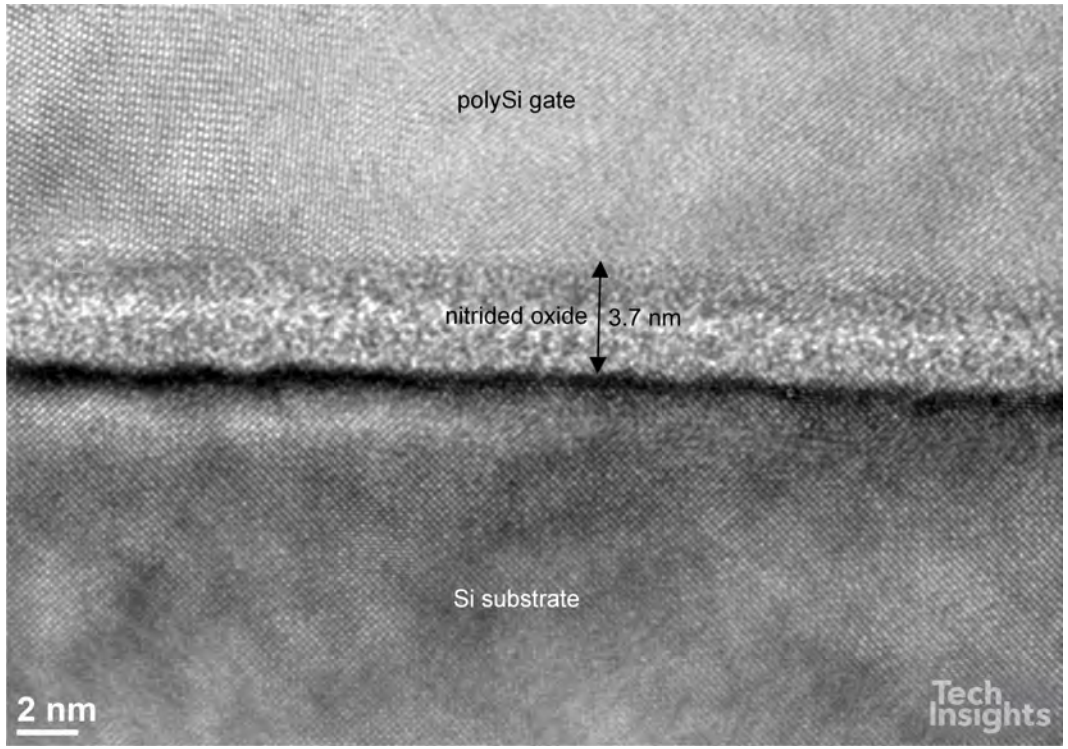


readout_large gates 27k_399150.png

Readout Circuitry Longer Transistors Detail – TEM

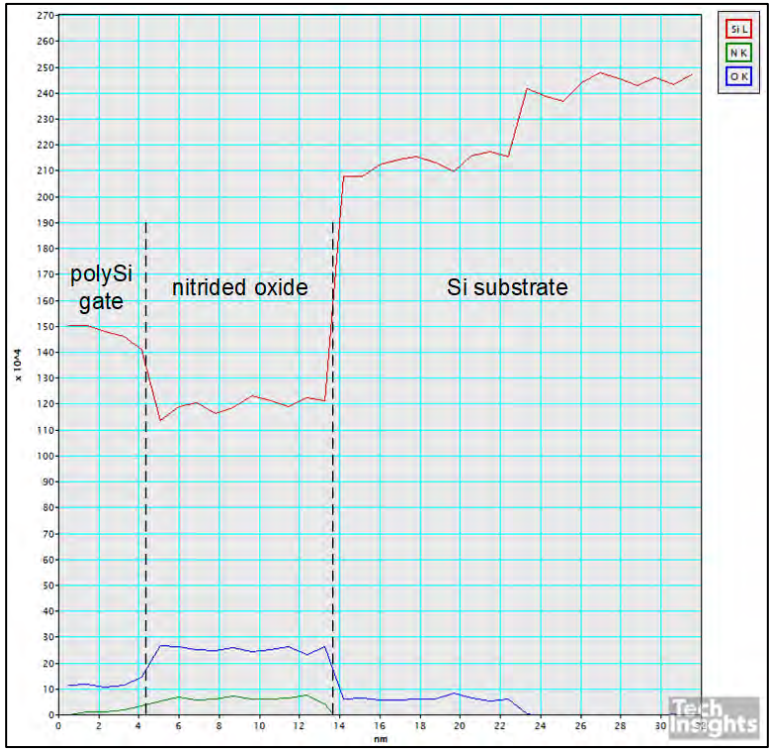
Readout Circuitry Transistors

- TEM and TEM-EELS images showing the gate dielectric of the readout circuitry longer transistor.
- The longer transistor gate dielectric is 3.7 nm thick nitrided oxide.



large gate dielectric 620k c_rc_399150.png

Readout Circuitry Transistor Gate Dielectric – TEM



113508_EELS line scan_large gate dielectric_399150.png

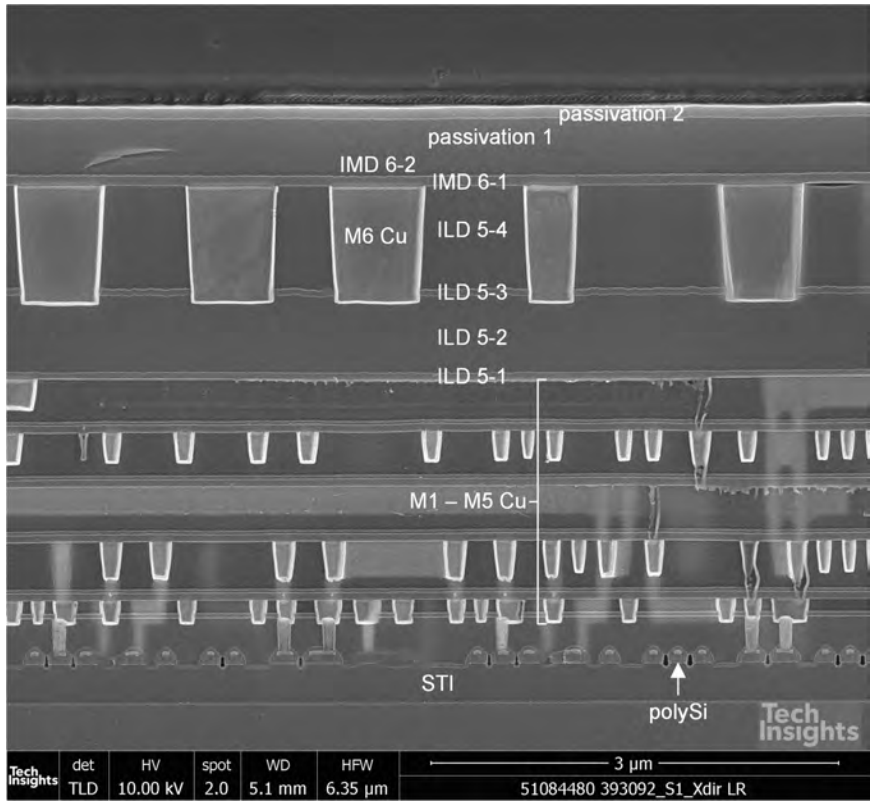
Readout Circuitry Transistor Gate Dielectric – TEM-EELS

FEOL and BEOL Logic Region

Tech Insights

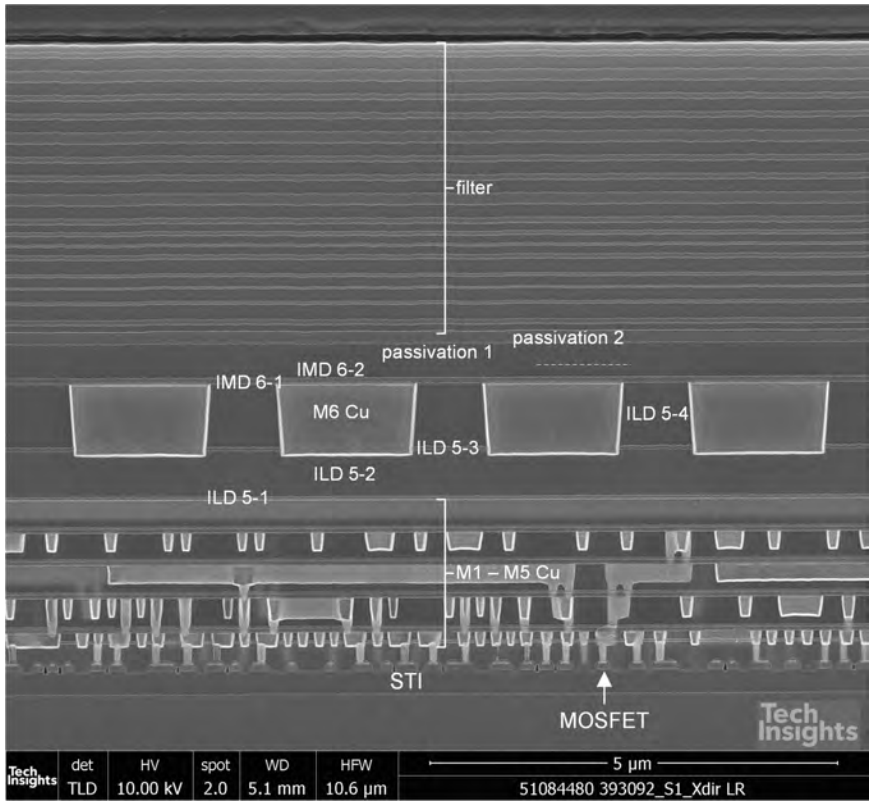
Logic Transistors

- SEM cross section images showing the general structure in the logic region.
- The PMD and ILD layers in the logic region are the same as in the SPAD array, with exception of ILD 5-4 (full layer thickness) and metal 6.
- Some logic circuitry regions have the multilayer filter above the passivation layer, and some do not.



578_General_Structure_393092.png

Logic Region Overview – SEM

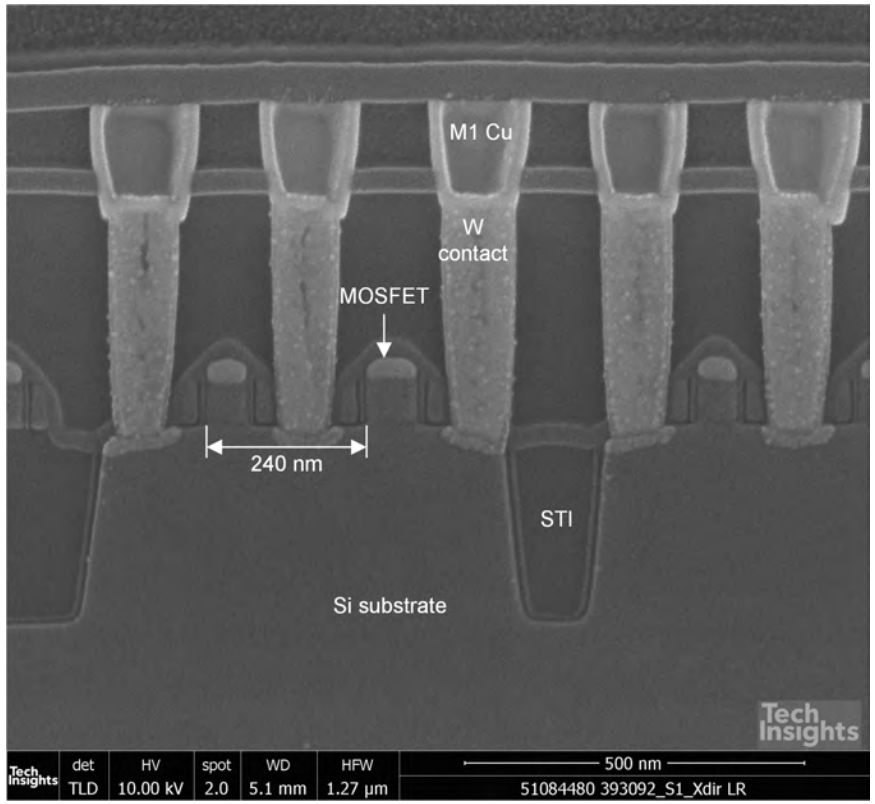


584_General_Structure_393092.png

Logic Region Overview – SEM

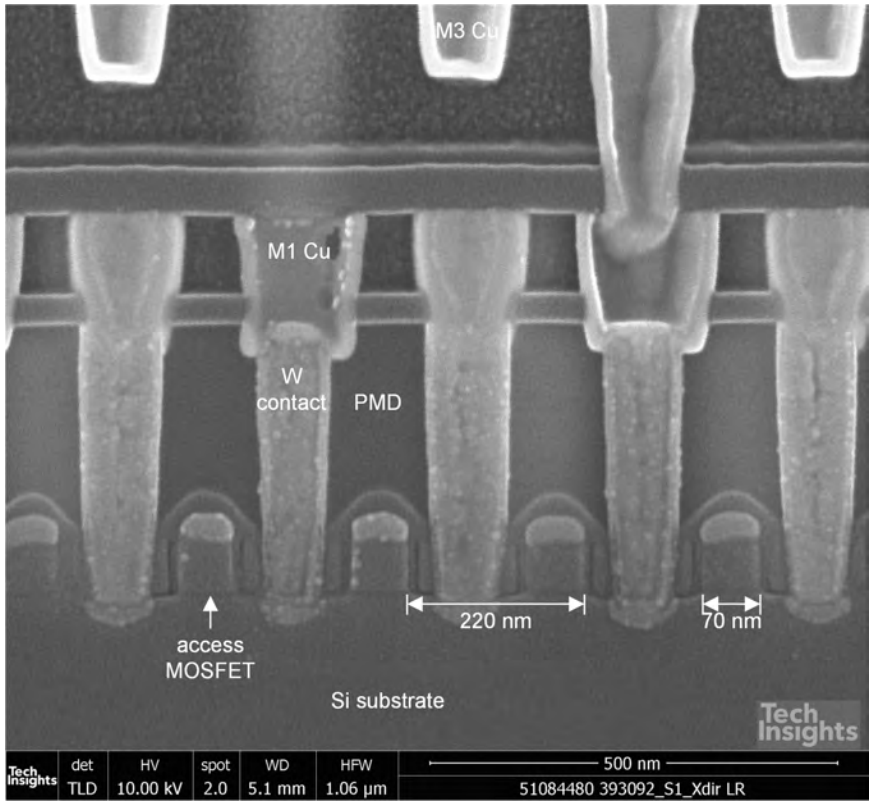
Logic Transistors

- The minimum logic gate contacted gate pitch observed was 240 nm.
- However, the SRAM memory has the smallest contacted gate pitch (220 nm) observed in the entire die; though, the gate length (70 nm) is larger.



587_Lower_Structure_393092_1.png

Logic Minimum Contacted Gate Pitch – SEM

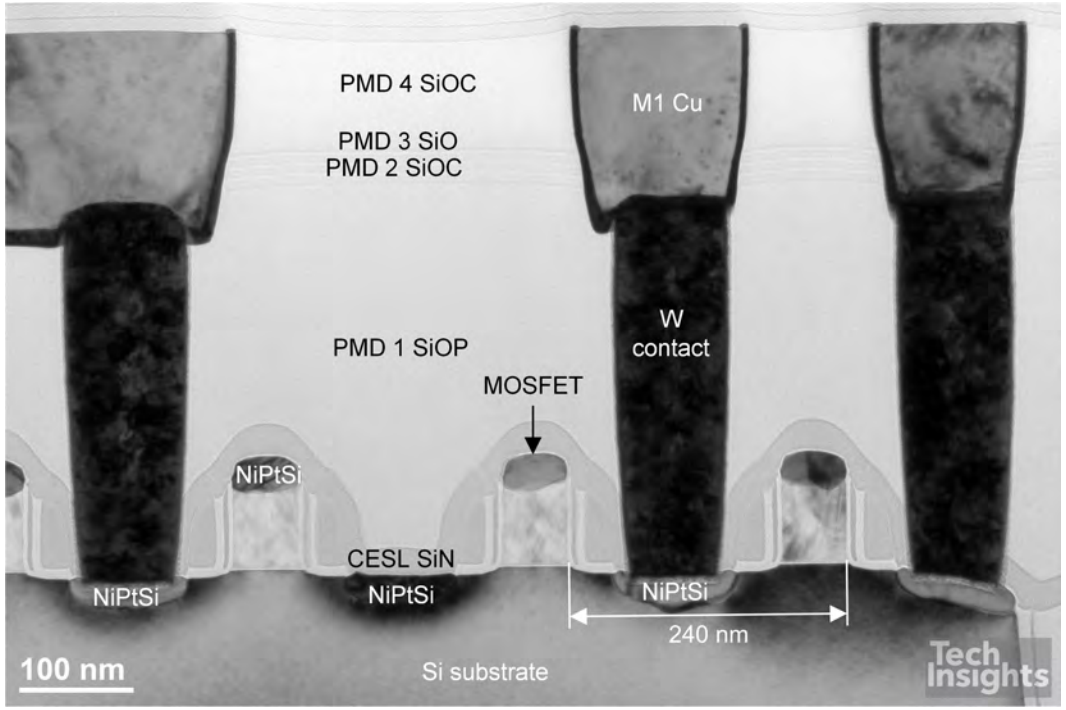


568_SRAM_NMOS_393092.png

SRAM Minimum Contacted Gate Pitch – SEM

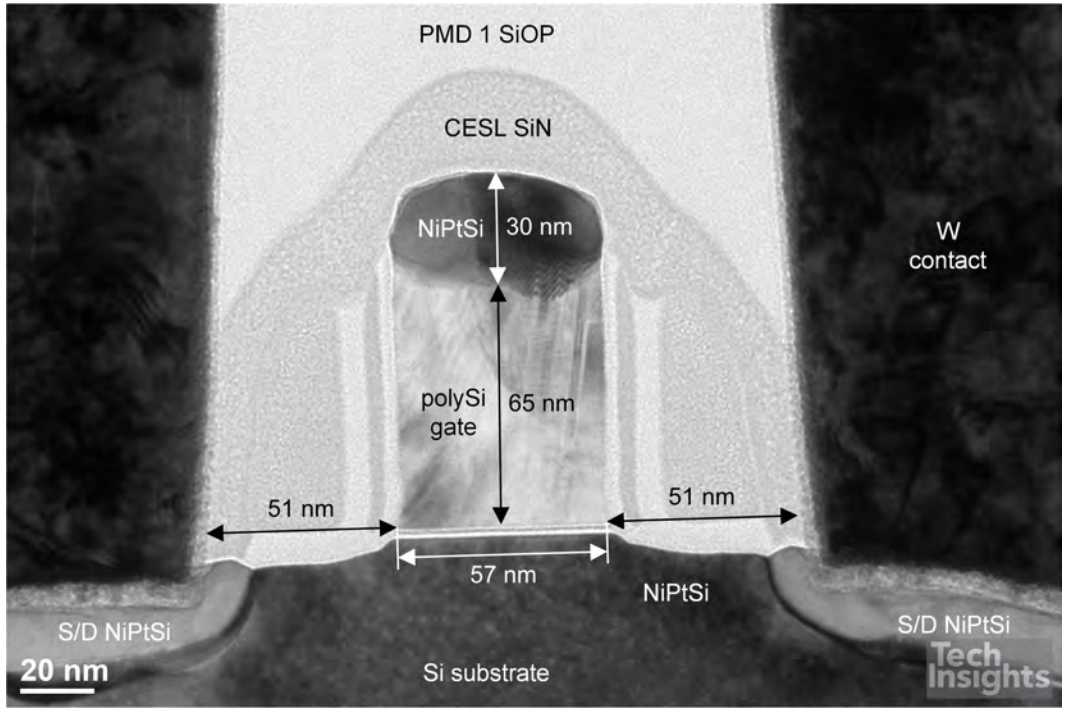
Logic Transistors

- The minimum contacted gate pitch observed in the logic transistor is 240 nm and the minimum metal pitch is 180 nm (see page 90). Based on these critical dimensions and observed process features, the SPAD die was likely manufactured by ams OSRAM in a 65 nm CMOS process node.
- The polySi gate and S/D regions use NiPtSi, and the transistor length is 57 nm, which is the same as the minimum contacted gate pitch observed in the SPAD readout circuitry.



logic 27k g_397216.png

Logic Transistor Overview – TEM

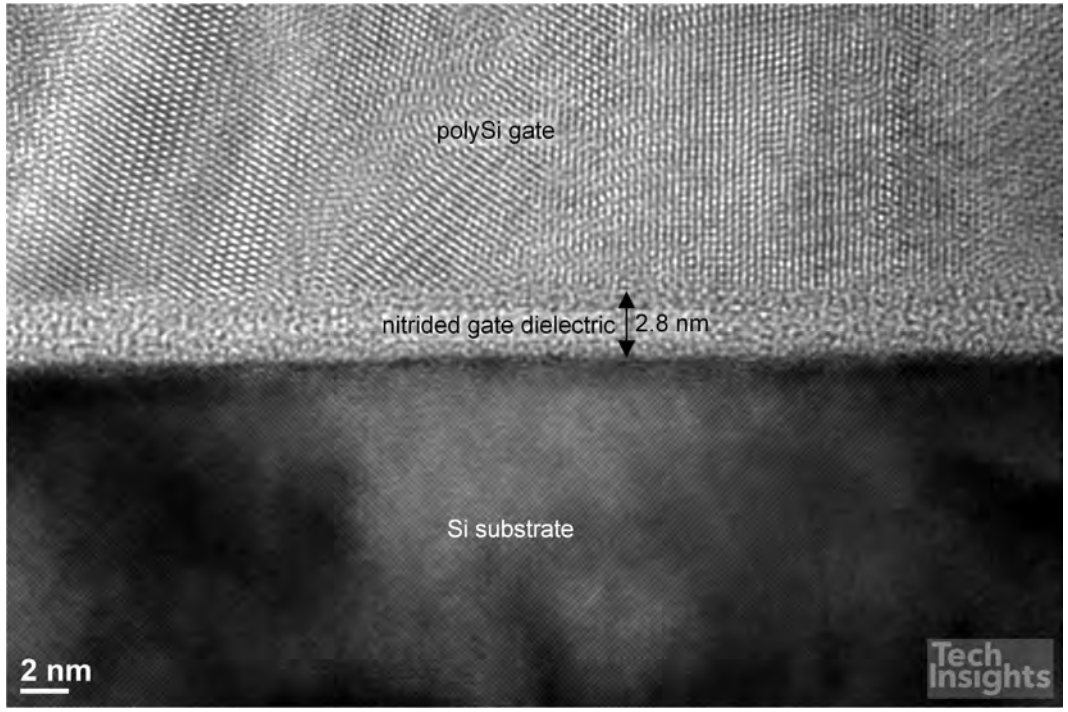


logic gate 88k g_397216.png

Logic Transistor Detail – TEM

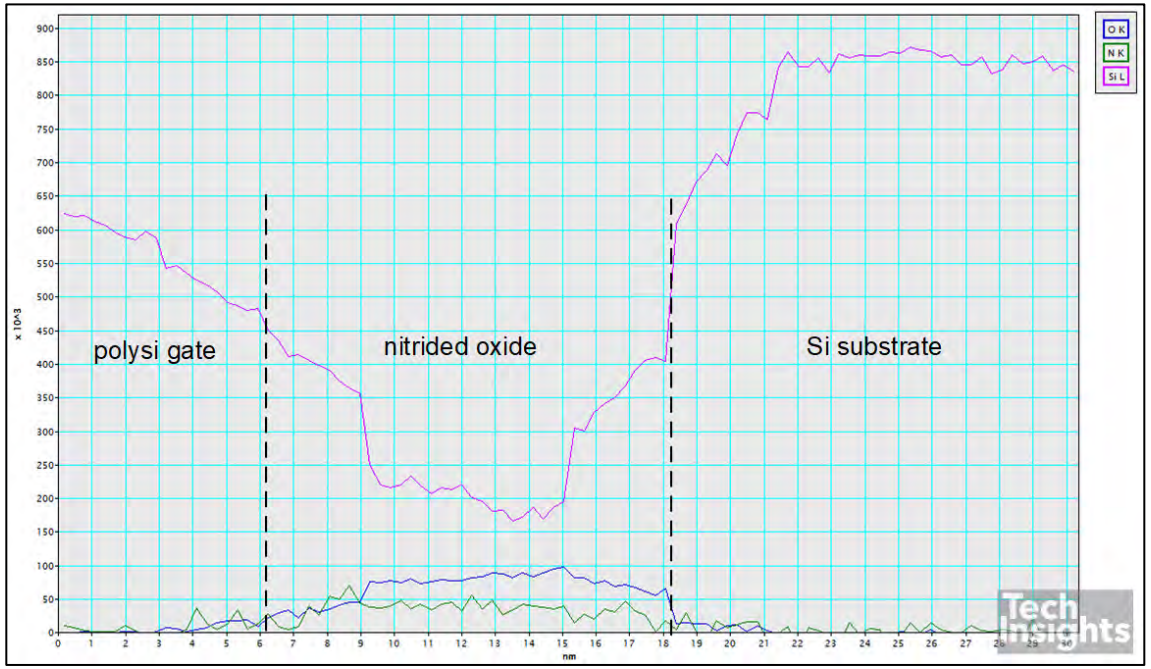
Logic Transistors

- TEM and TEM-EELS images showing the logic transistor gate dielectric.
- The logic transistor gate dielectric is 2.8 nm thick nitrided oxide.



logic gate dielectric 530k_397216.png

Logic Transistor Gate Dielectric – TEM

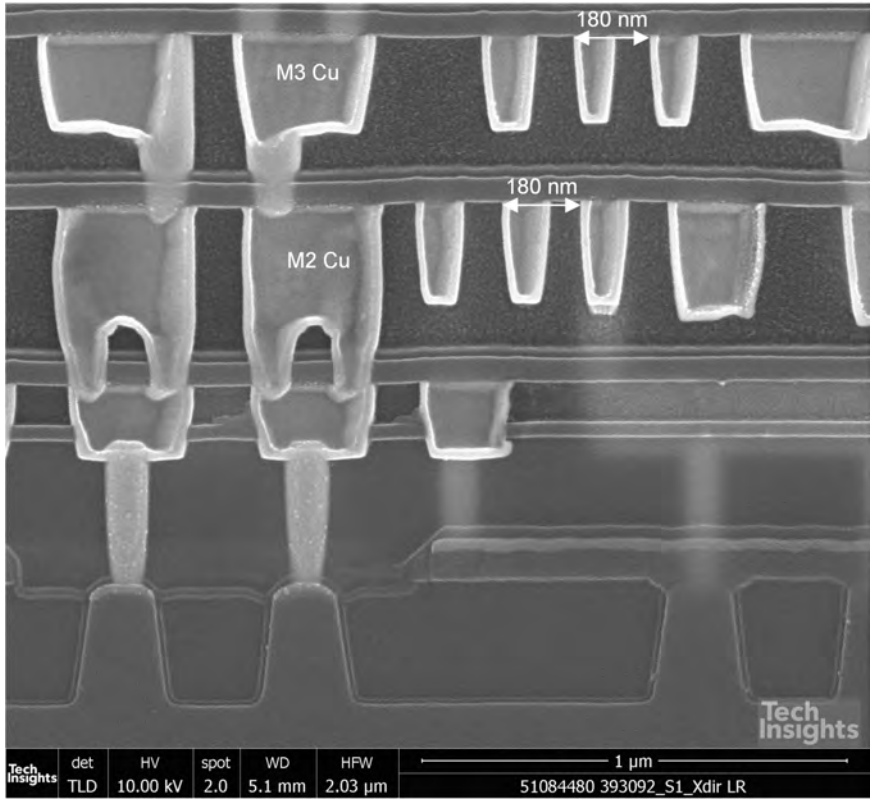


132225_EELs line scan_logic gate dielectric_397216.png

Logic Transistor Gate Dielectric – TEM-EELS

Logic Region Minimum Metal Pitch

- The minimum metal pitch in the logic region of 180 nm was observed on metal 2 and metal 3.

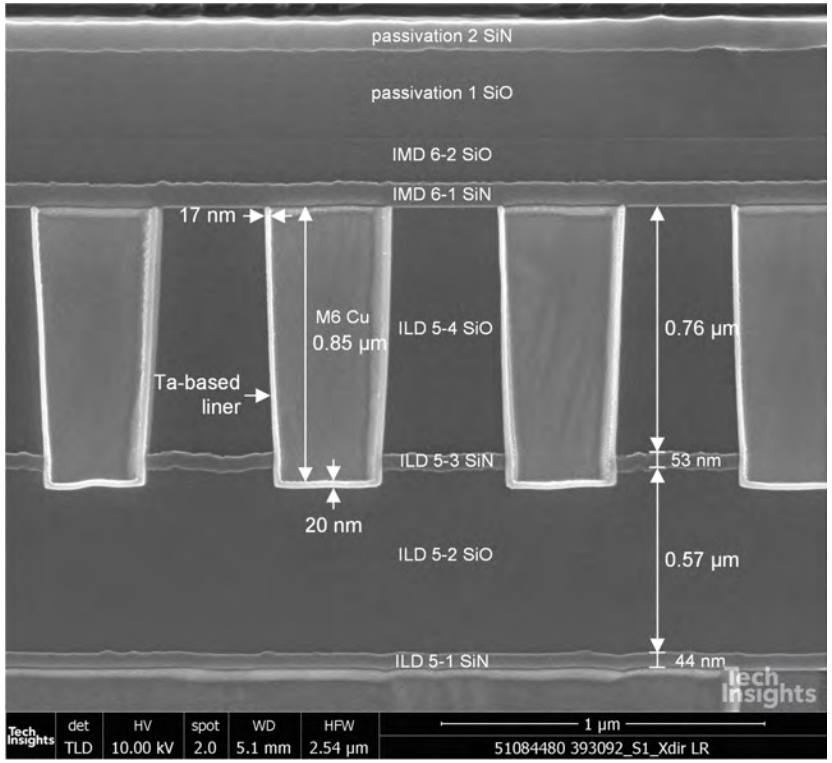


565_Lower_Structure_393092.png

Minimum Metal Pitch – SEM

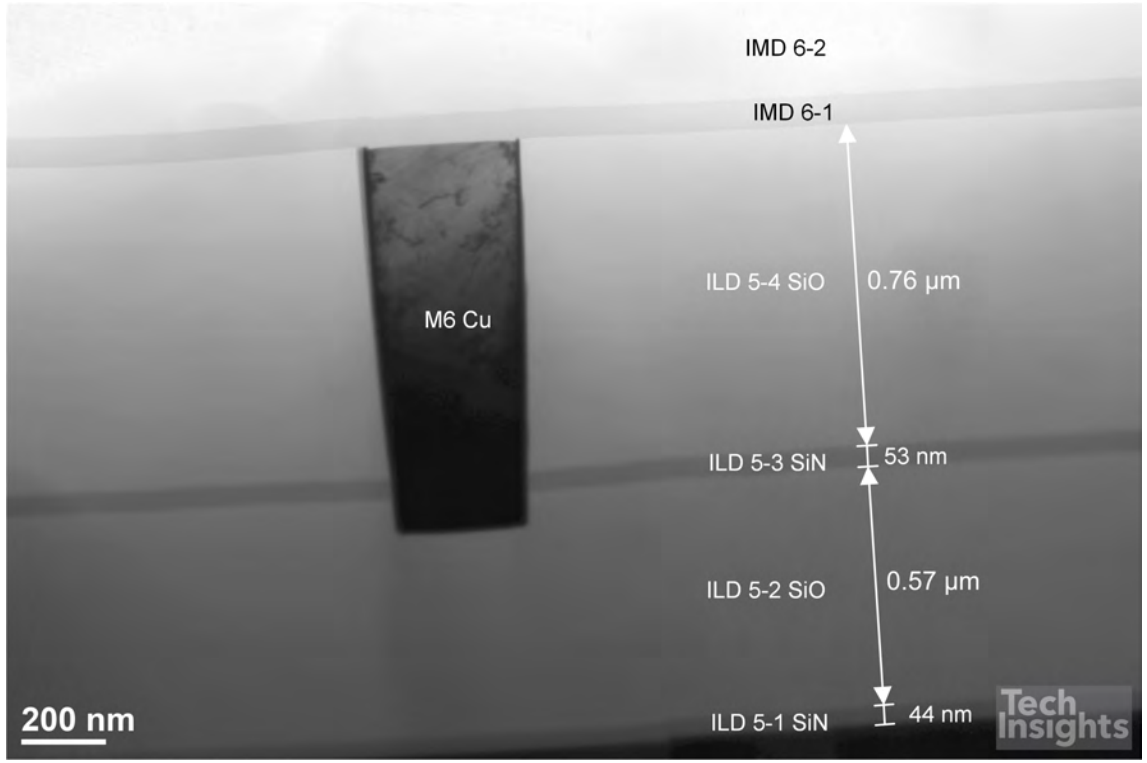
Logic Region ILD 5 and Metal 6

- ILD 5 comprises a 44 nm thick ILD 5-1 nitride, a 0.57 µm thick ILD 5-2 oxide, a 53 nm thick ILD 5-3 nitride, and a 0.76 µm thick ILD 5-4 oxide.
- Metal 6 is a 0.85 µm thick dual Cu damascene with a 20 nm thick Ta-based liner.



573_M6_393092.png

ILD 5 and Metal 6 – SEM

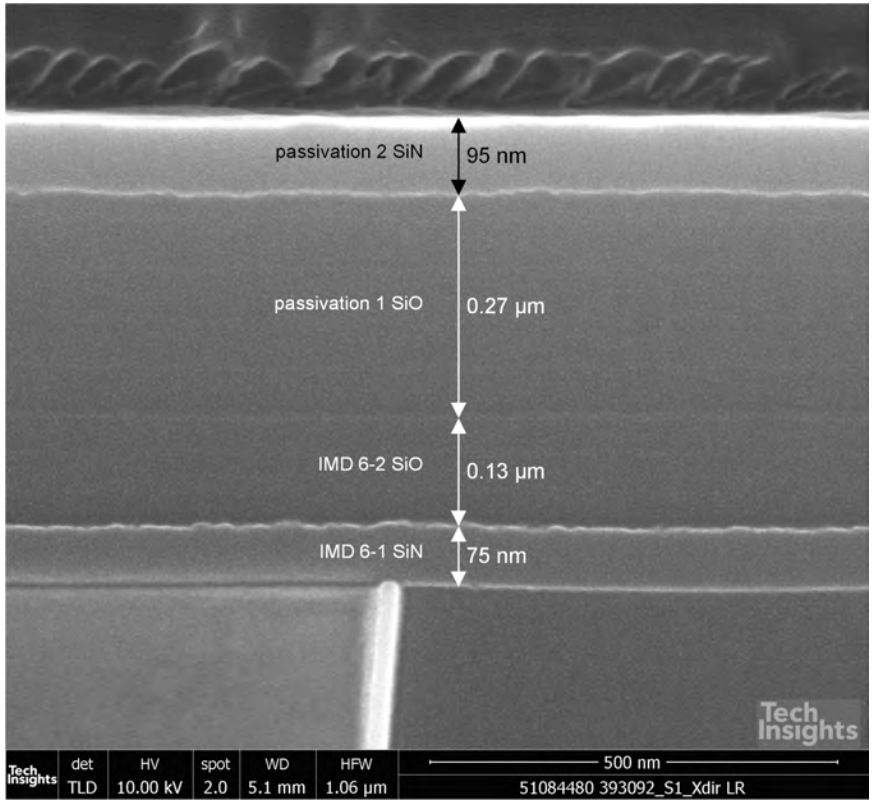


metal 6 9k_397187.png

ILD 5 and Metal 6 – TEM

Logic Region IMD 6 and Passivation

- The top layers of IMD 6 (IMD 6-3 and IMD 6-4) were etched in the logic region and most of the periphery during the metal 7 Al etch.
- In the logic region, IMD 6 comprises a 75 nm thick IMD 6-1 nitride and a thinned 0.13 µm thick IMD 6-2 oxide.
- The passivation comprises a 0.27 µm thick passivation 1 oxide and a 95 nm thick passivation 2 oxide.



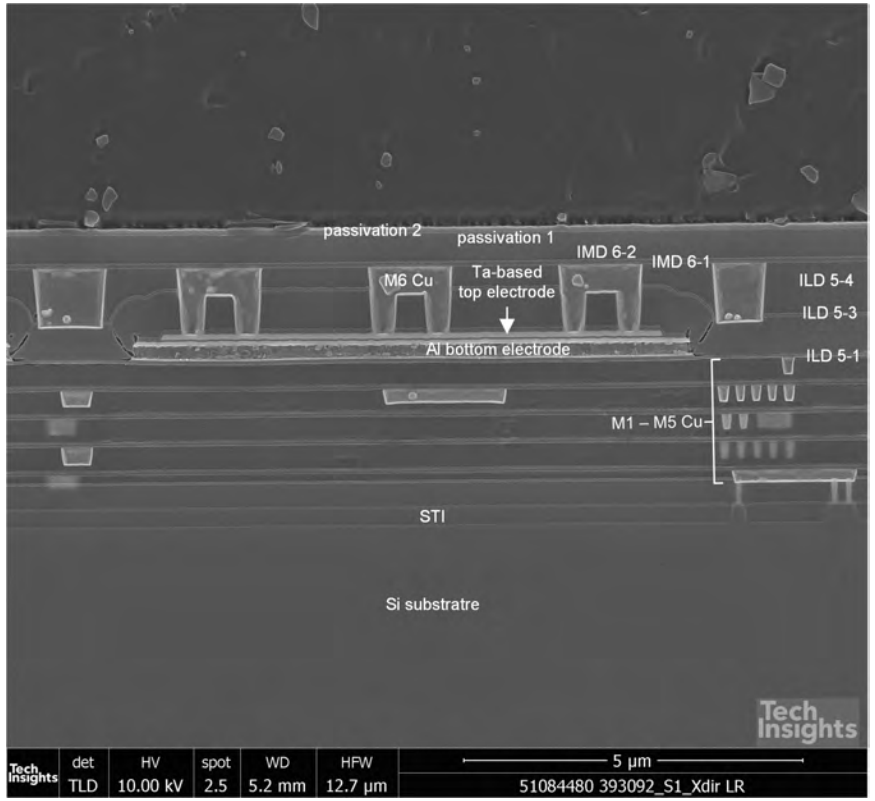
561_Peripheral_Passivation_393092.png

IMD 6 and Passivation – SEM

Periphery Region

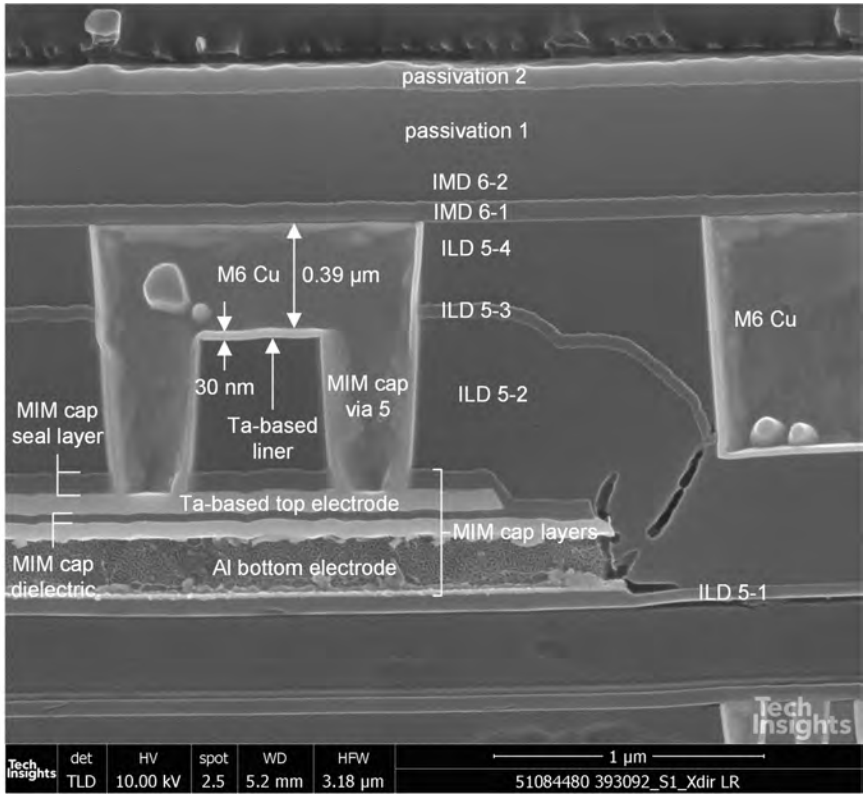
Periphery Region – MIM Capacitor

- MIM capacitors were observed in the periphery region between metal 5 and metal 6.
- Metal 6 connected to the MIM capacitor top electrode is thinner (0.39 µm) than the regular metal 6 thickness (0.76 µm).



801_MIM_Cap_393092.png

MIM Capacitor Overview – SEM

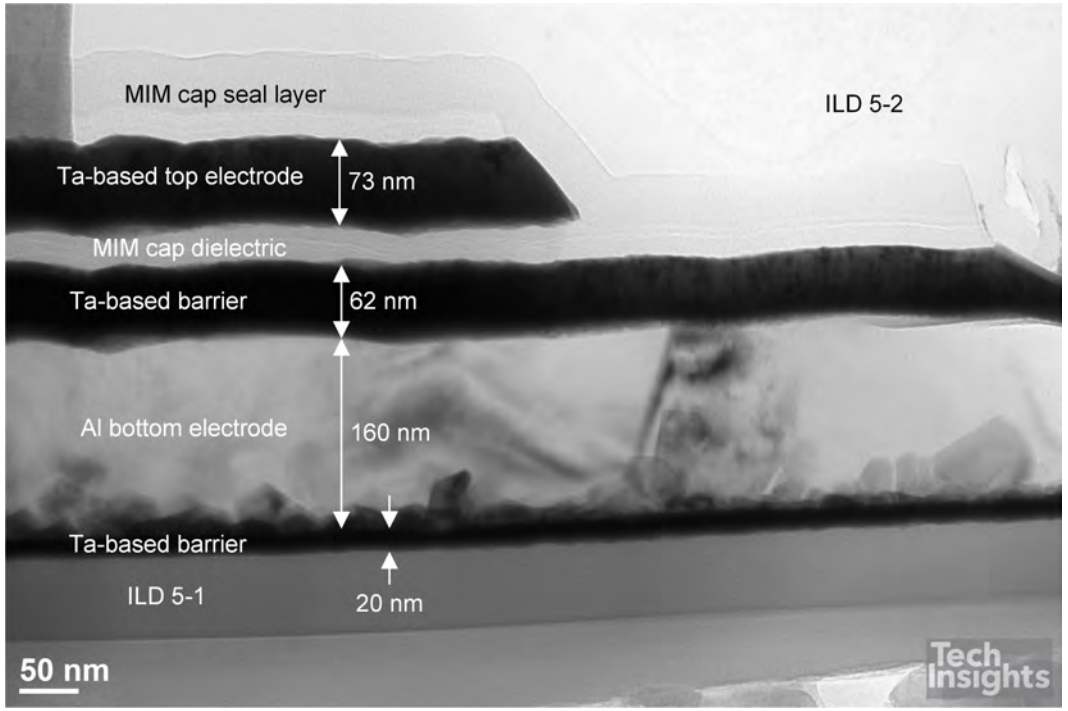


802_MIM_Cap_393092.png

MIM Capacitor Detail – SEM

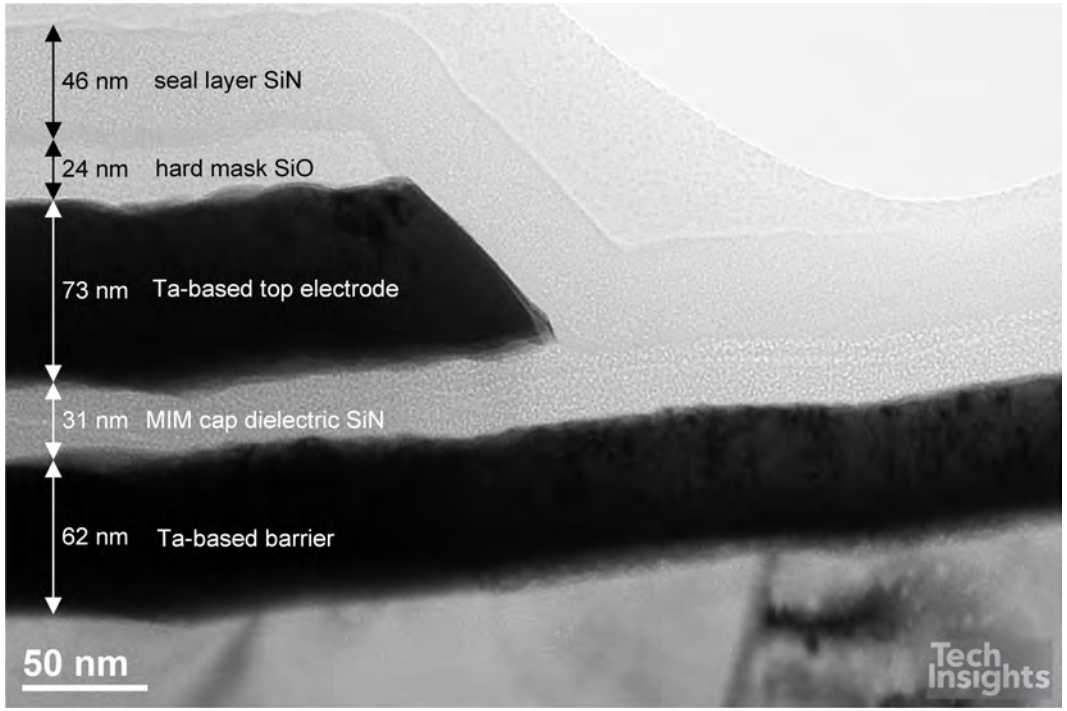
Periphery Region – MIM Capacitor

- TEM cross section detail images showing the MIM capacitors electrodes, dielectric, and seal layers.
- The bottom electrode comprises a 20 nm thick bottom metal barrier, a 160 nm thick Al body, and a 62 nm thick Ta-based top metal barrier.
- The dielectric is a 31 nm thick nitride, and the top electrode is a 73 nm thick Ta-based layer.
- A 24 nm thick oxide hardmask was used to define the top electrode, and a 46 nm thick nitride was used to seal the MIM capacitor.



mims caps other edge 27k_399357.png

MIM Capacitor Detail – TEM

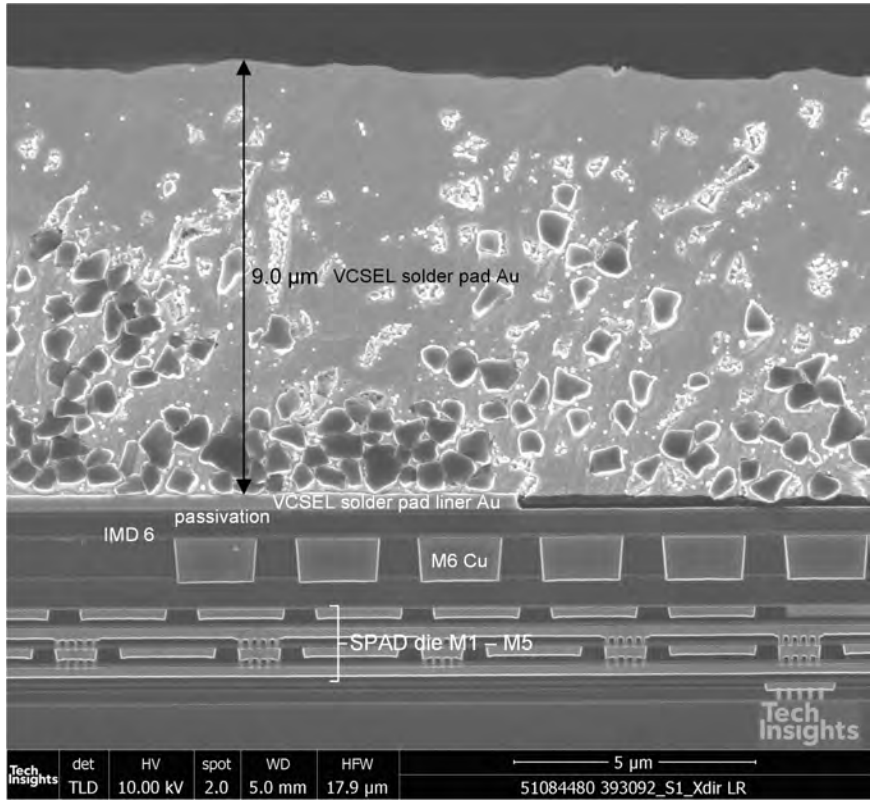


mims caps other edge 64k g1_399357.png

MIM Capacitor Detail – TEM

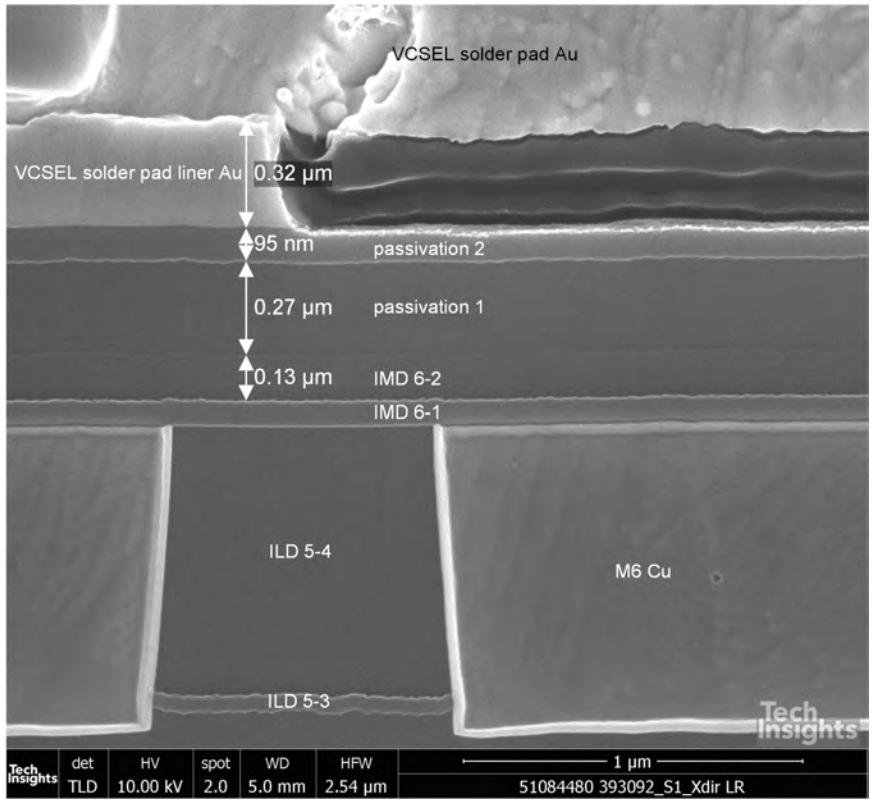
Periphery Region – VCSEL Solder Pad

- SEM cross section overview and close-up images in the VCSEL region.
- A VCSEL solder pad comprising an Au liner and body was formed after the SPAD fabrication was complete, likely as part of the assembly process.
- The VCSEL solder pad is about 9 µm thick and the liner is 0.32 µm thick.



645_Region_Bellow_VCSEL_General_Structure_393092.png

VCESL Solder Pad Overview – SEM

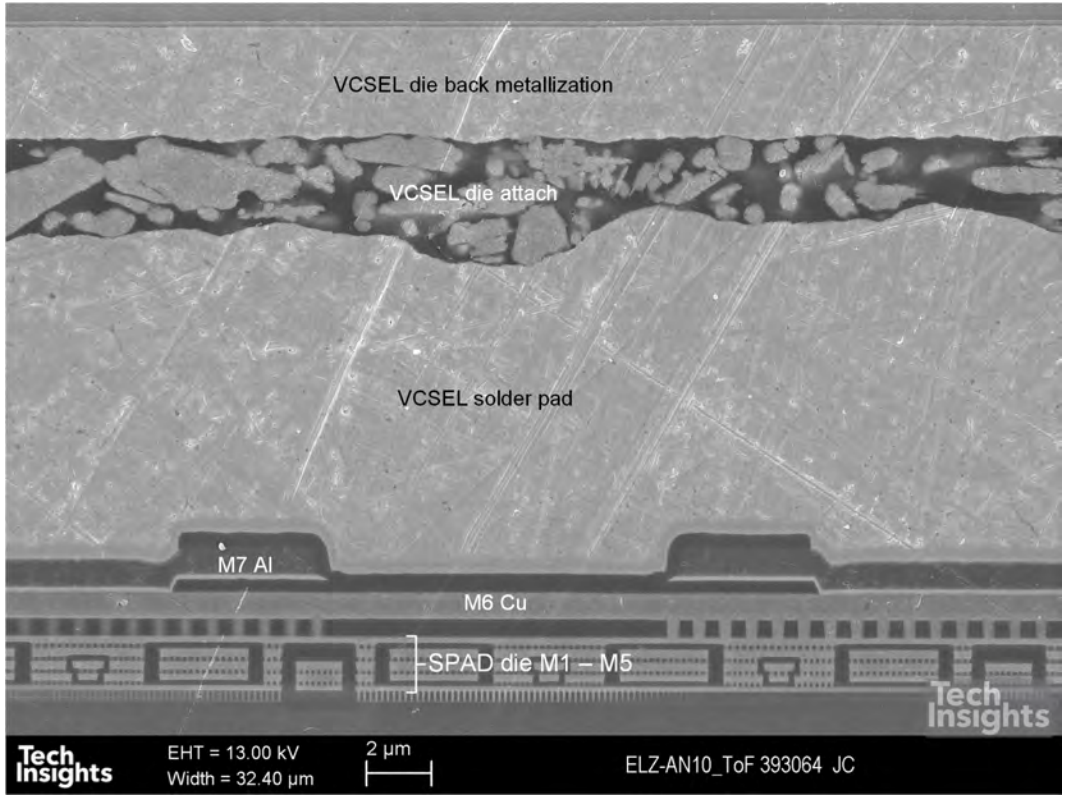


650_Region_Bellow_VCSEL_Die_393092.png

VCESL Solder Pad Close-Up – SEM

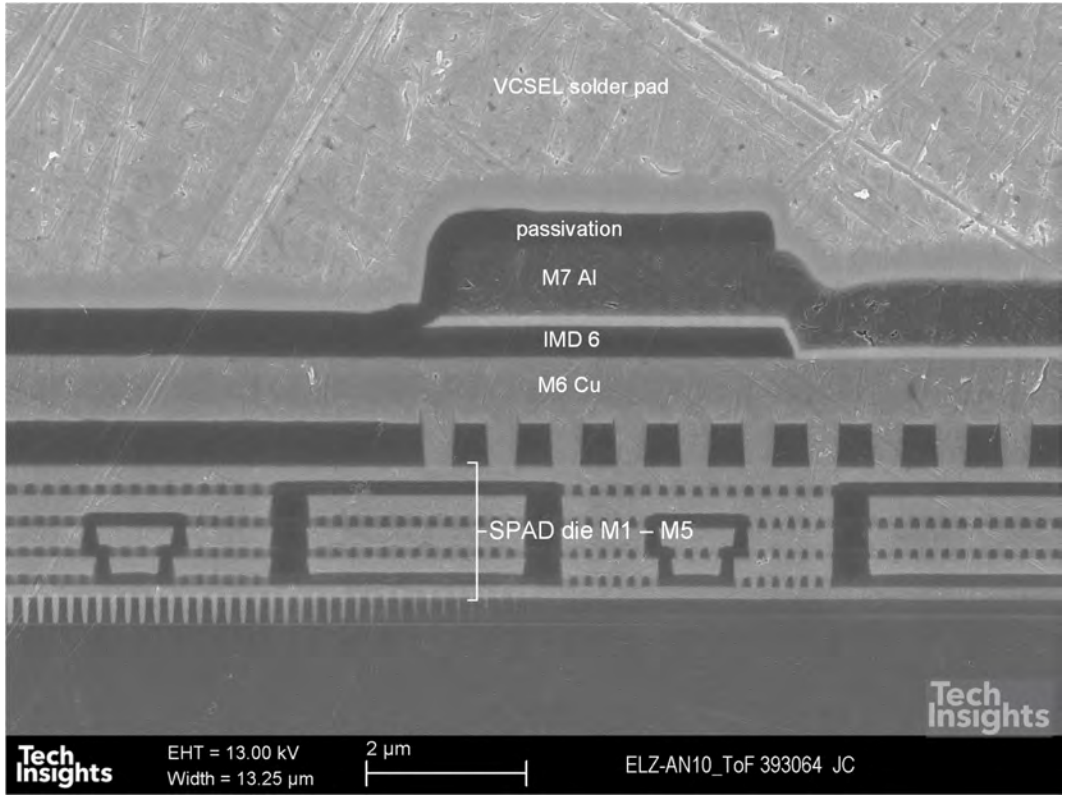
Periphery Region – VCSEL Solder Pad

- SEM cross section overview and close-up images in the VCSEL bond pad region.
- The VCSEL solder pad connects to SPAD die metal 7 Al.



23 LED attach_393064.png

VCESL Solder Pad Overview – SEM

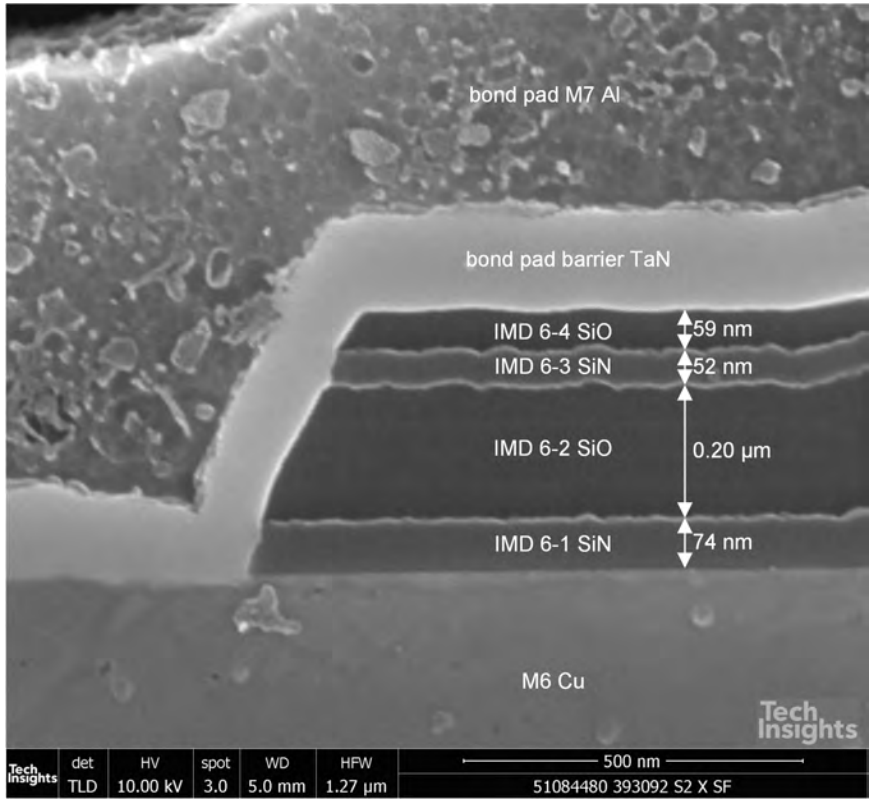


24 general structure_393064.png

VCESL Solder Pad Close-Up – SEM

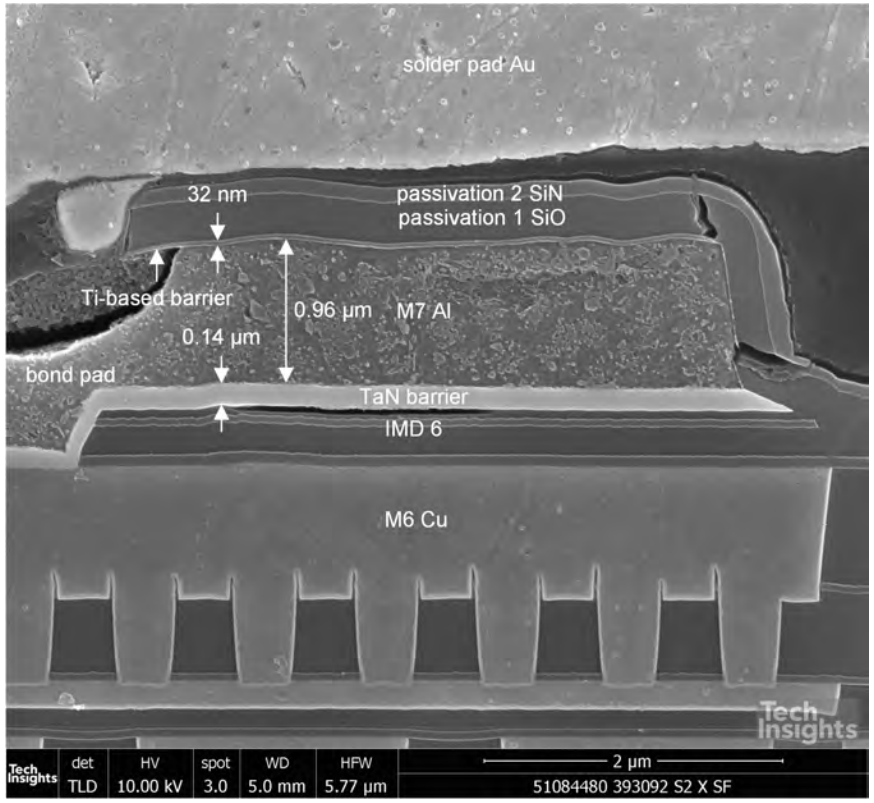
Periphery Region – IMD 6 and Metal 7

- SEM cross section image showing IMD 6 and metal 7 in the periphery region.
- IMD 6 comprises a 74 nm thick IMD 6-1 nitride, a 0.20 µm thick IMD 6-2 oxide, a 52 nm thick IMD 6-3 nitride, a 59 nm thick IMD 6-4 oxide.
- Metal 7 comprises a 0.14 µm thick TaN barrier, a 0.96 µm thick Al body, and 32 nm thick Ti-based barrier.



012_bond_pad_393092.png

IMD 6 – SEM



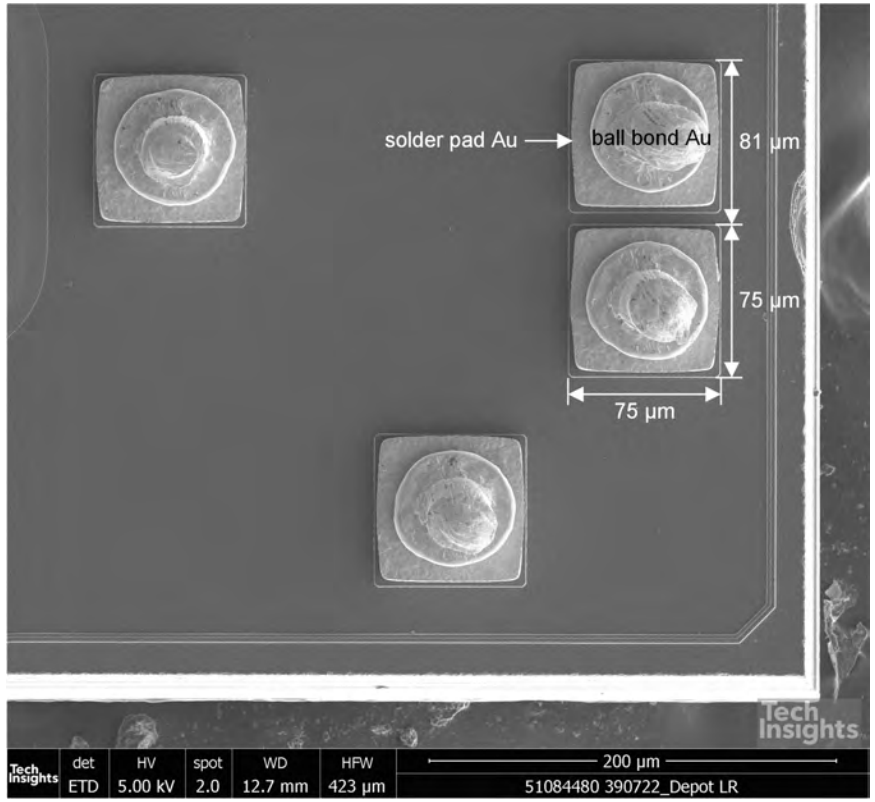
010_bond_pad_393092.png

Metal 7 – SEM

Bond Pad

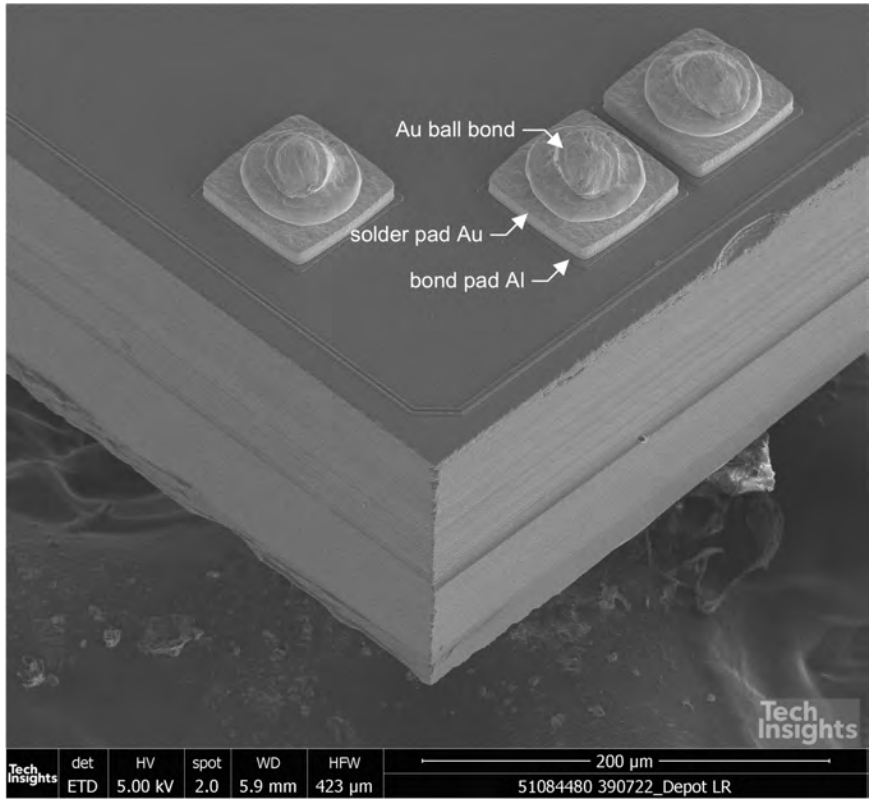
Bond Pads

- The minimum bond pad pitch is 81 µm. The bond pad is 75 µm × 75 µm.
- The bond wire is attached to the Au solder pad, formed over the Al bond pad.



106_51084480_CornerC_390722.png

Bond Pad Minimum Pitch – SEM Plan-View

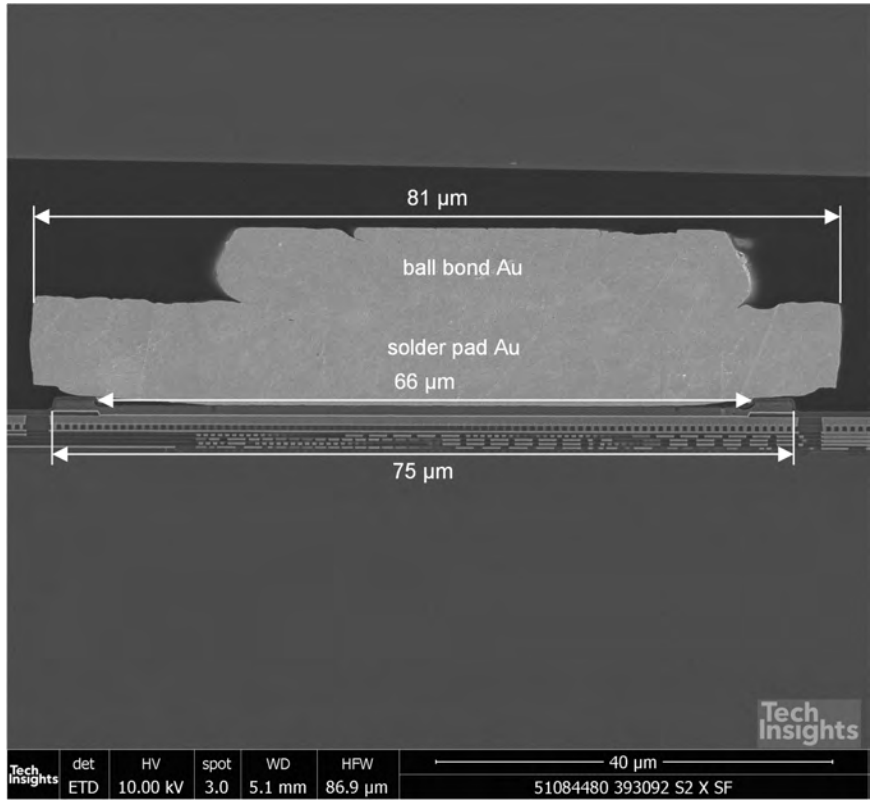


127_CornerC_Tilt_390722.png

Bond Pad Pitch – SEM Tilt-View

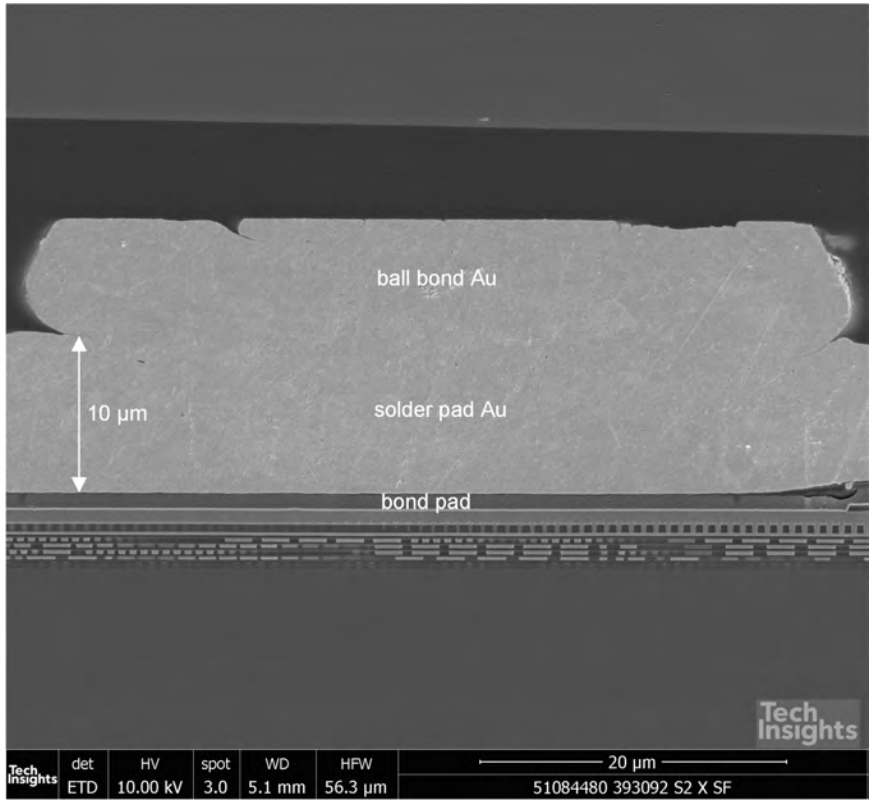
Bond Pads

- The bond pad is 75 µm wide.
- The passivation opening is 66 µm wide.
- The Au solder pad is 81 µm wide and 10 µm thick, including the liner.



002_bond_pad_393092.png

Bond Pad Overview – SEM

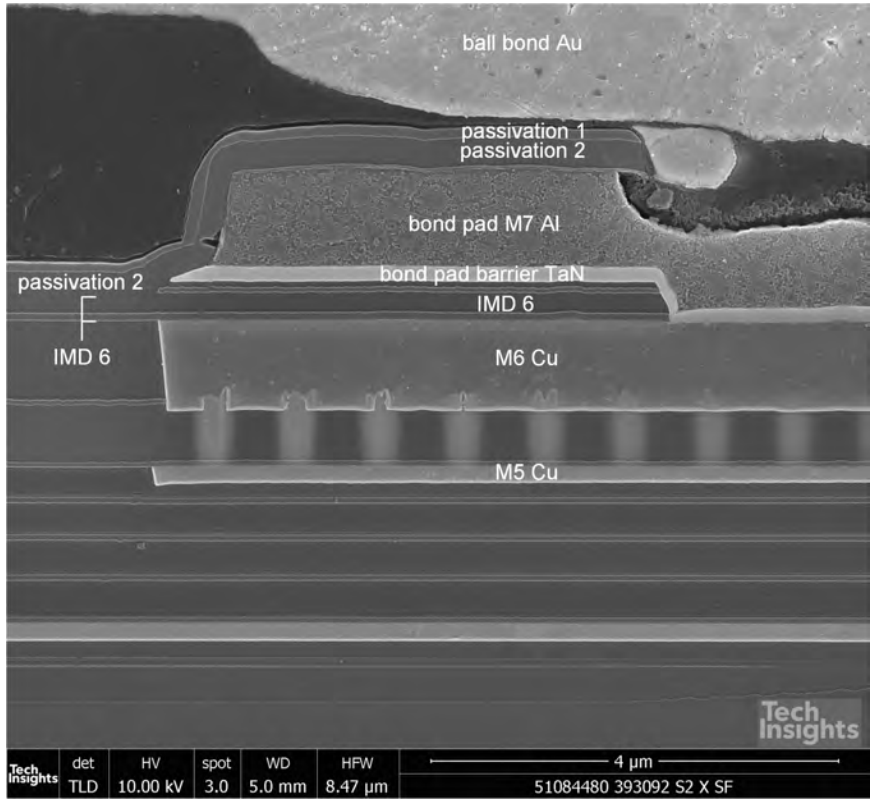


017_bond_pad_393092.png

Bond Pad Close-Up – SEM

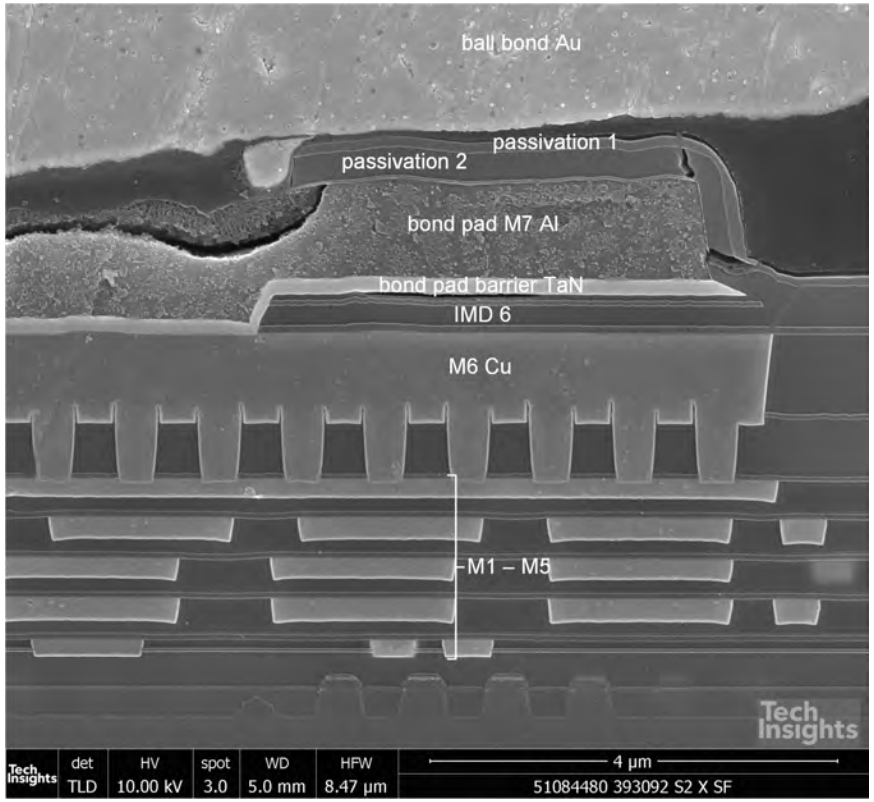
Bond Pads

- SEM cross section images showing the bond pad edges.
- The regions where metal 7 Al was etched, IMD 6-4 and IMD 6-3 were etched away.



004_bond_pad_393092.png

Bond Pad Edge – SEM

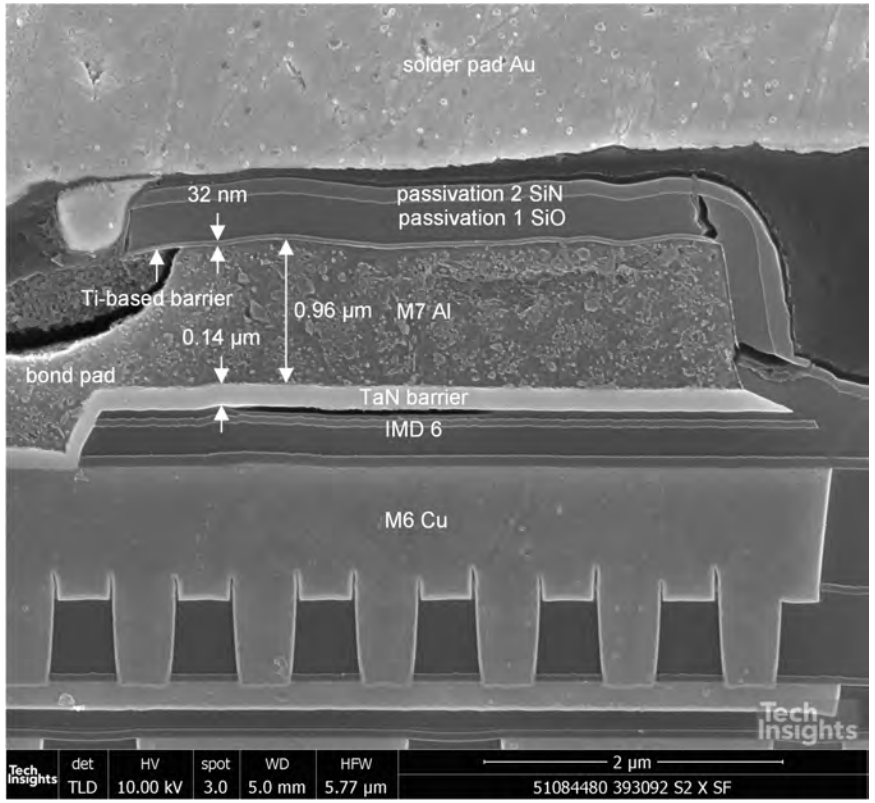


009_bond_pad_393092.png

Bond Pad Edge – SEM

Bond Pads

- The bond pad comprises a 0.14 µm thick TaN barrier, a 0.96 µm thick metal 7 Al body and 32 nm thick Ti-based barrier.



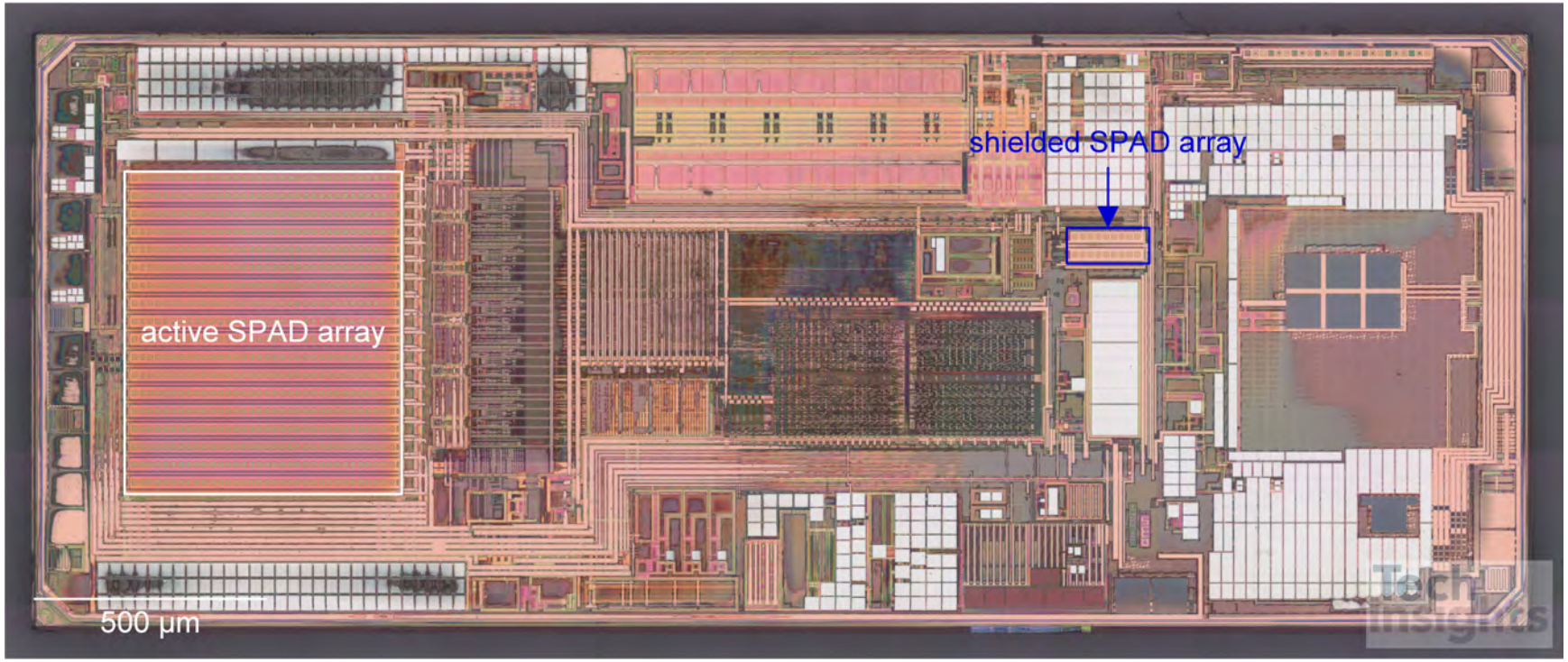
010_bond_pad_393092.png

Bond Pad Edge – SEM

SPAD Plan-View Analysis

SPAD Array Planar Analysis

- SPAD die optical image at metal 6.
- The active and shielded SPAD arrays are annotated.

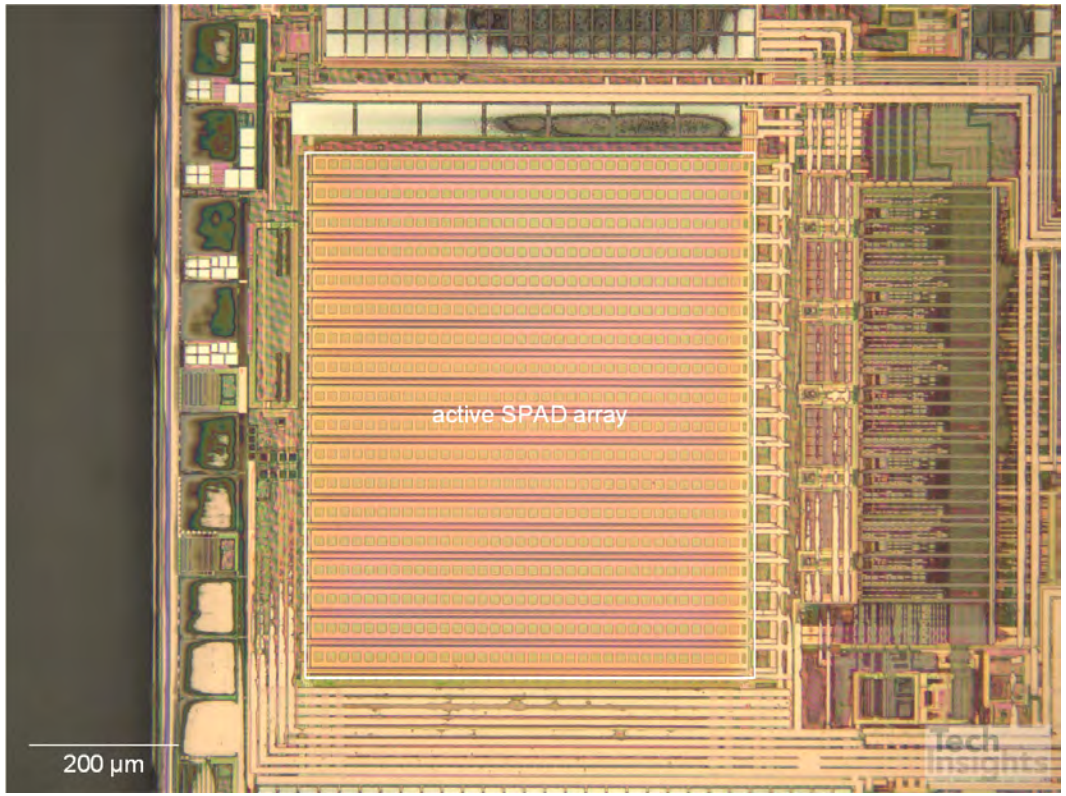


ELZ-AN20_ToF_51084480_391407_M6_1.png

SPAD Die at Metal 6 – Optical

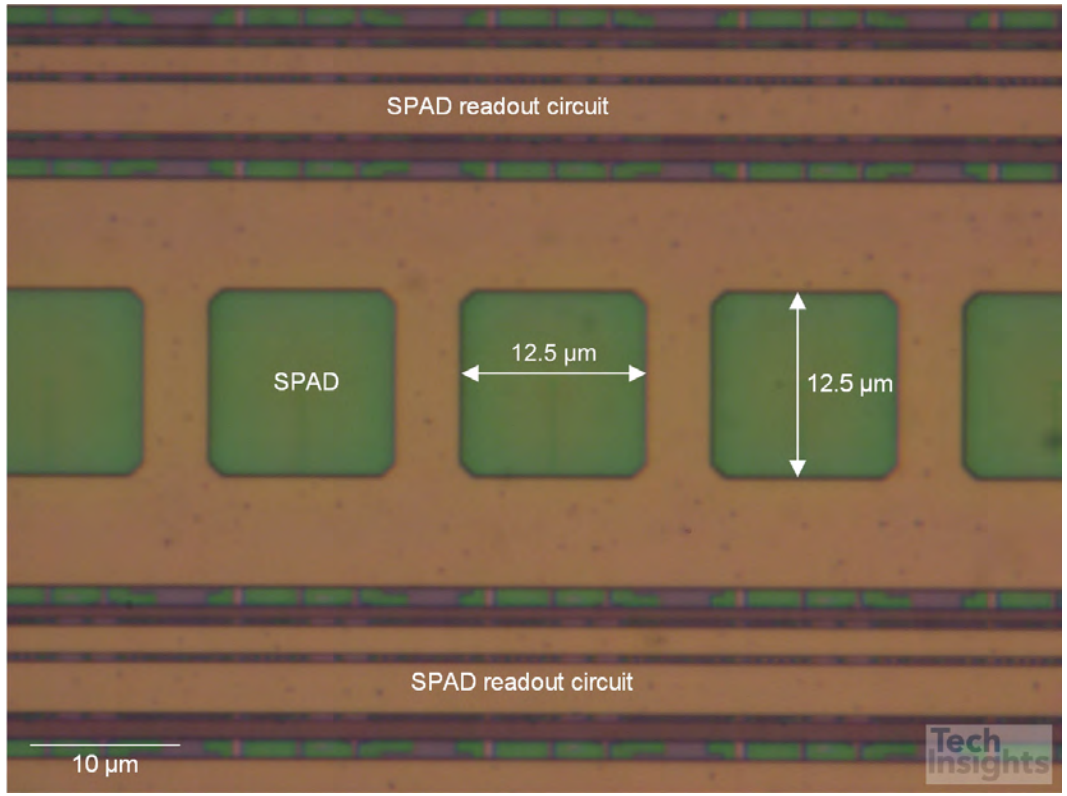
SPAD Array Planar Analysis

- Overview and close-up optical images of the active SPAD array
- The active SPAD array is organized in 18 rows by 34 columns (total 614 active SPADs). The SPAD rows are interleaved with rows of SPAD readout circuitry.



01 10x1r_391407.png

Active SPAD Array Overview – Optical

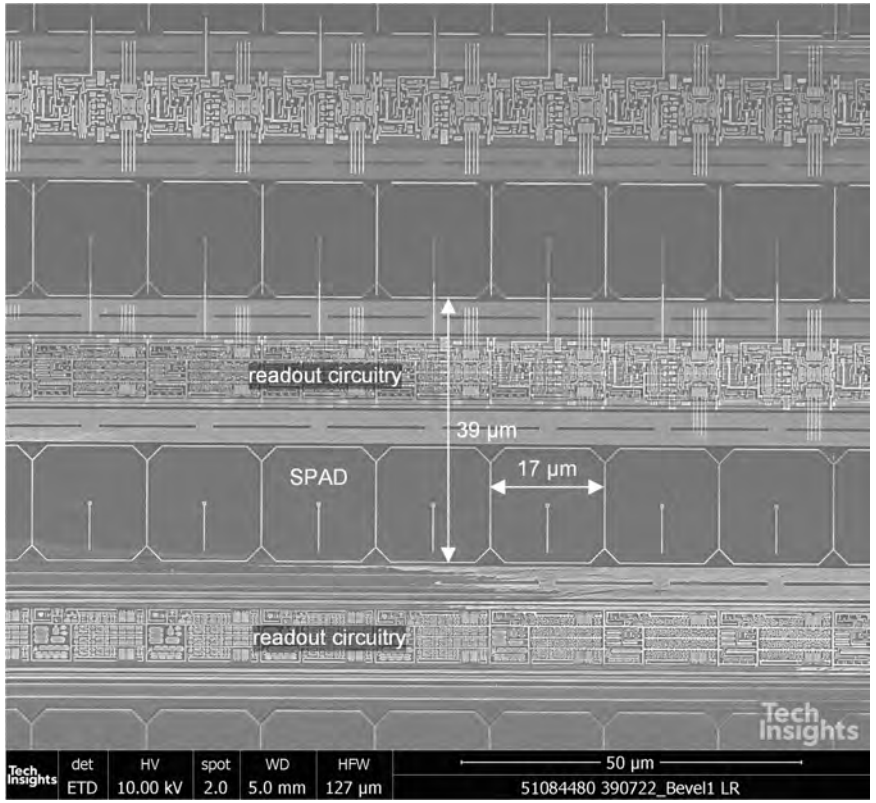


05 100x2r_391407.png

Active SPAD Array Close-Up – Optical

SPAD Array Planar Analysis

- SEM plan-view overview image of the active SPAD array, showing the SPAD and readout circuitry.
- The SPAD pixel has a vertical pitch of 39 µm, which includes the SPAD and the readout circuitry, and a horizontal pitch of 17 µm between adjacent SPADs.

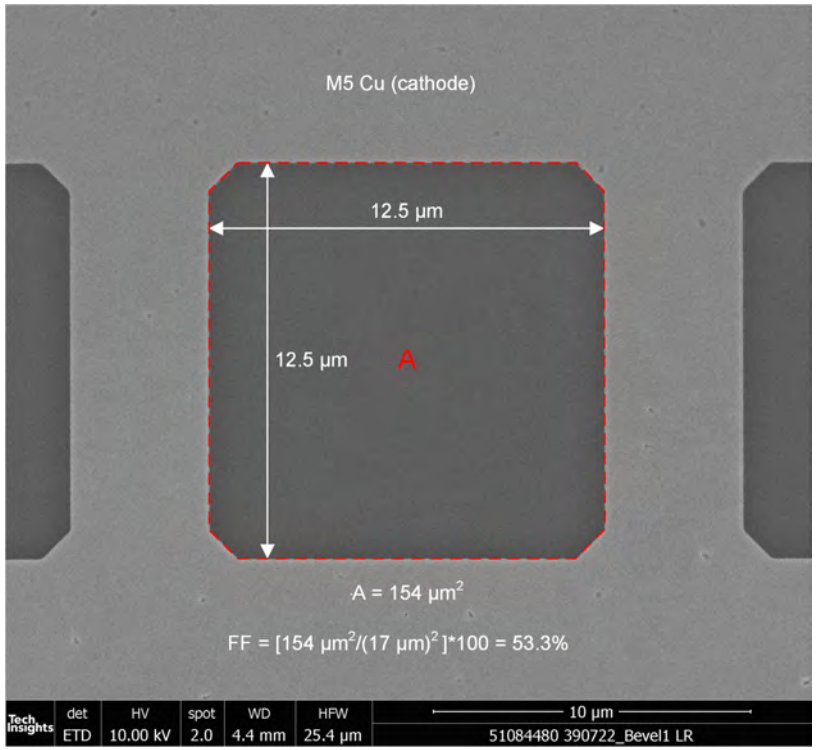


230_Bevel1_Array_390722.png

Active SPAD Pitch – SEM Plan-View

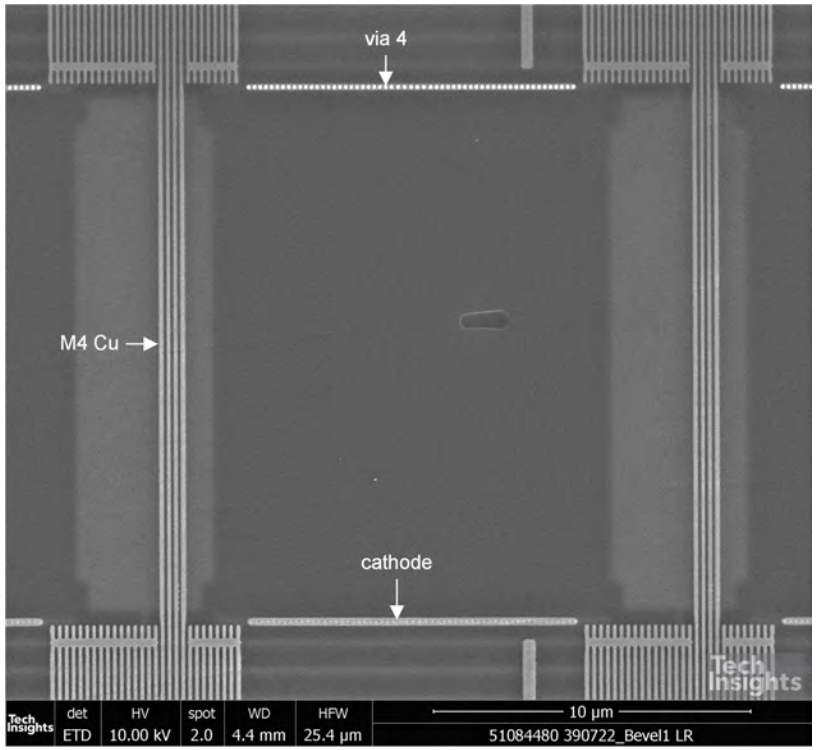
SPAD Array Planar Analysis

- The active SPAD at metal 5 showing the SPAD aperture grid width is connected to the cathode potential. The aperture FF is 53.3%, considering only the 17 µm × 17 µm SPAD.
- The active SPAD at metal 4 and via 4 showing the cathode interconnect.



360_Bevel1_Array_M5_390722.png

Active SPAD at Metal 5 – SEM Plan-View

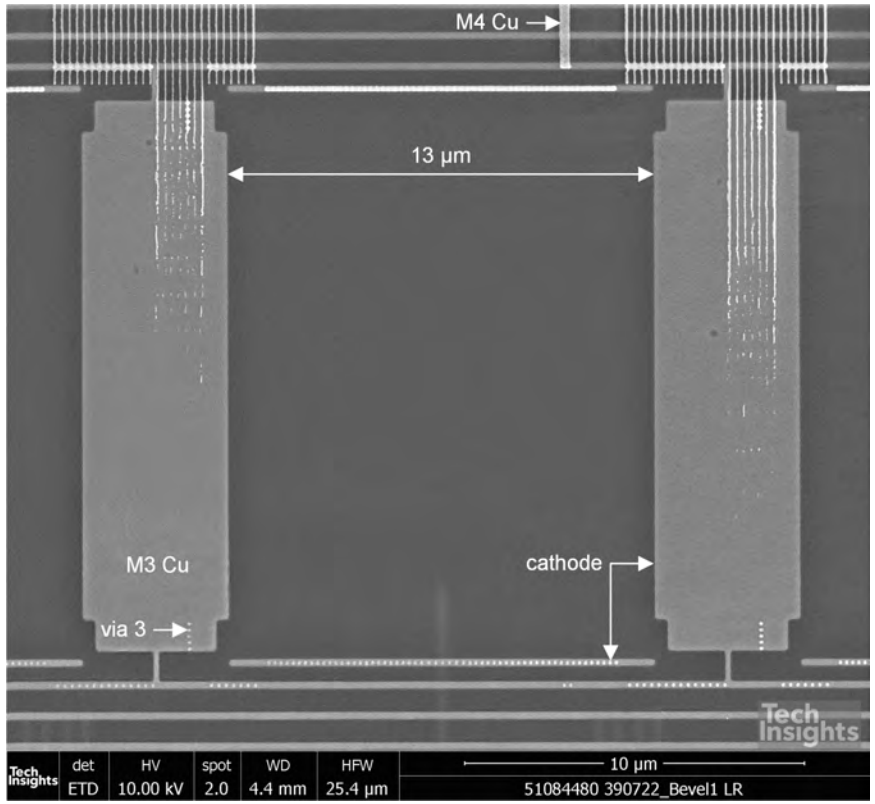


359_Bevel1_Array_M4_390722.png

Active SPAD at Metal 4 and Via 4 – SEM Plan-View

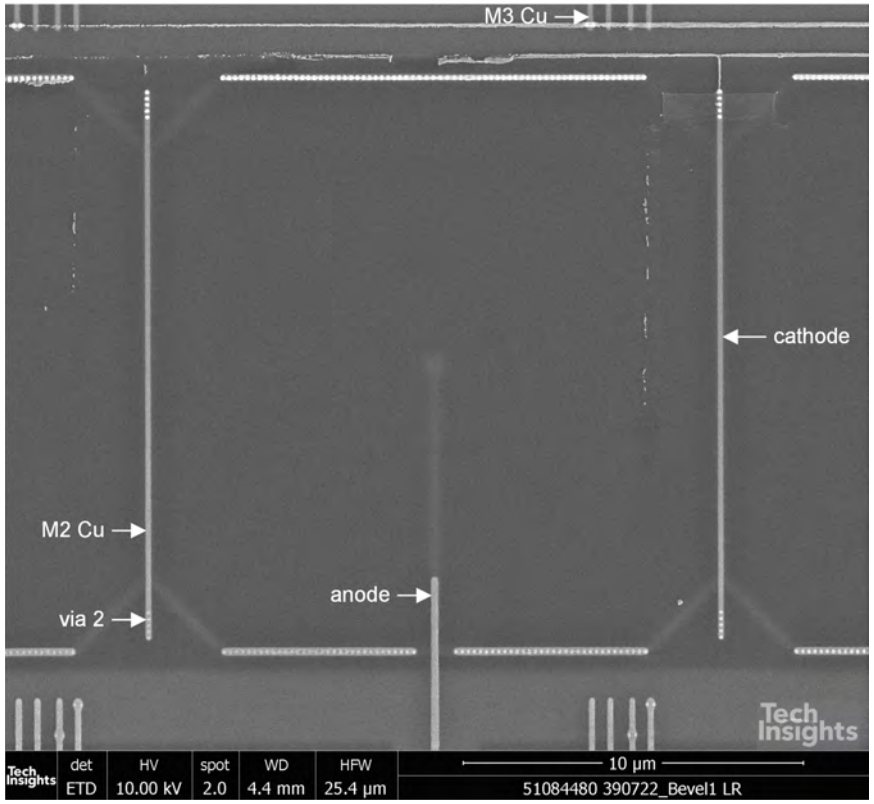
SPAD Array Planar Analysis

- The active SPAD at metal 3 and via 3 showing the cathode and anode interconnect.
- The active SPAD at metal 2 and via 2 showing the cathode and anode interconnect.



358_Bevel1_Array_M3_390722.png

Active SPAD at Metal 3 and Via 3 – SEM Plan-View

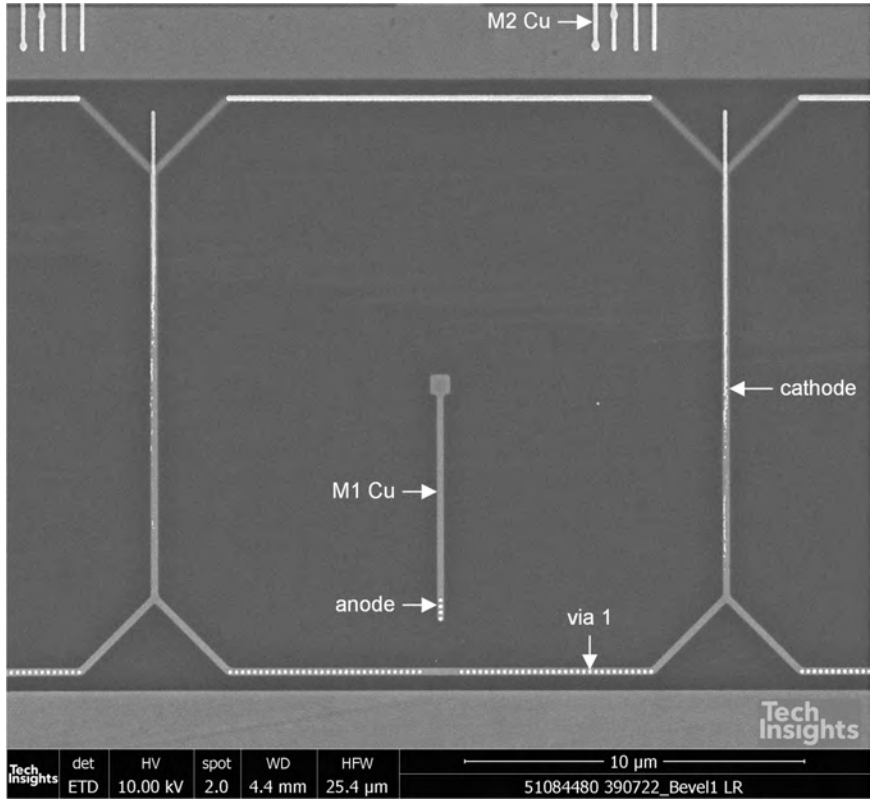


357_Bevel1_Array_M2_390722.png

Active SPAD at Metal 2 and Via 2 – SEM Plan-View

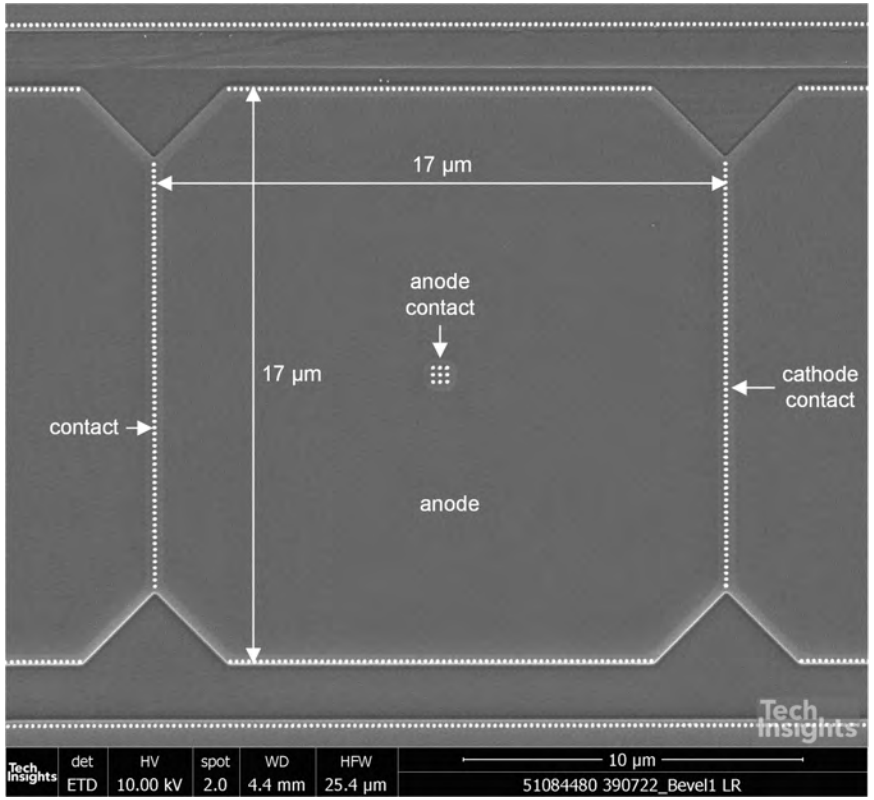
SPAD Array Planar Analysis

- The active SPAD at metal 1 showing the routing of the anode and the cathode interconnect.
- The active SPAD at contact shows nine anode contacts at the center and multiple cathode contacts at the SPAD boundaries. The active SPAD measures 17 µm x 17 µm.



356_Bevel1_Array_M1_390722.png

Active SPAD at Metal 1 and Via 1 – SEM Plan-View

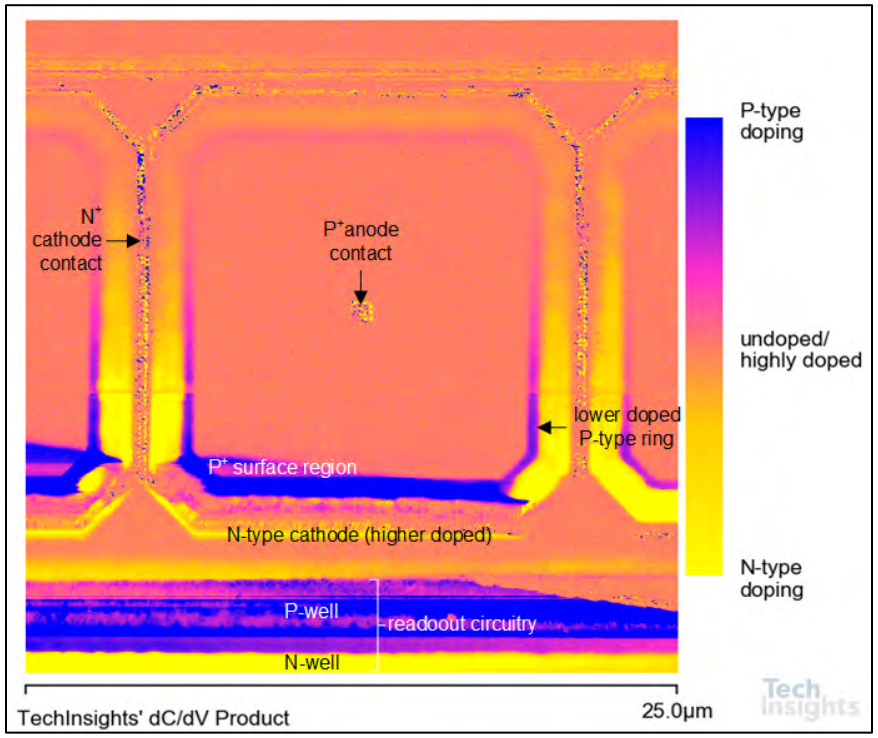


355_Bevel1_Array_Poly_390722.png

Active SPAD at Contact – SEM Plan-View

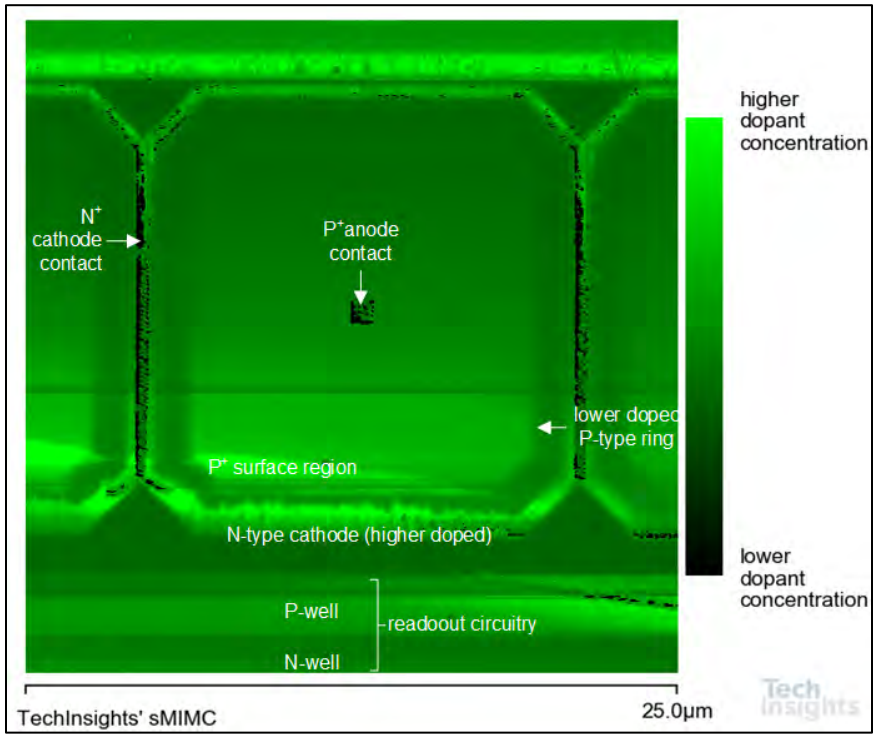
SPAD Planar Analysis

- SCM and SMIM-C images of the SPAD near the surface showing the anode and the cathode regions.
- The center region is the anode with a contact at the center. Near the surface the anode is surrounded by a lower doped type guard ring.
- The anode region closer to the surface is P^+ doped.



array_nearpoly_032422133833_PRODUCT_FRW_25.0u_512p_390722.png

SPAD Near the Surface – Planar SCM

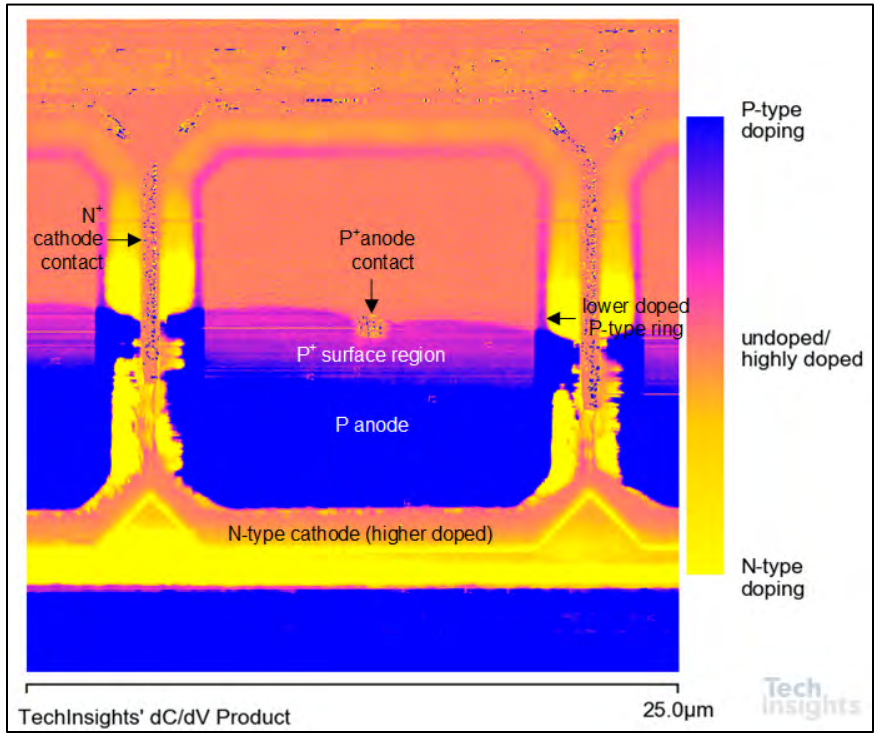


array_nearpoly_032422133833_SMIMC_FRW_25.0u_512p_390722.png

SPAD Near the Surface – Planar SMIM-C

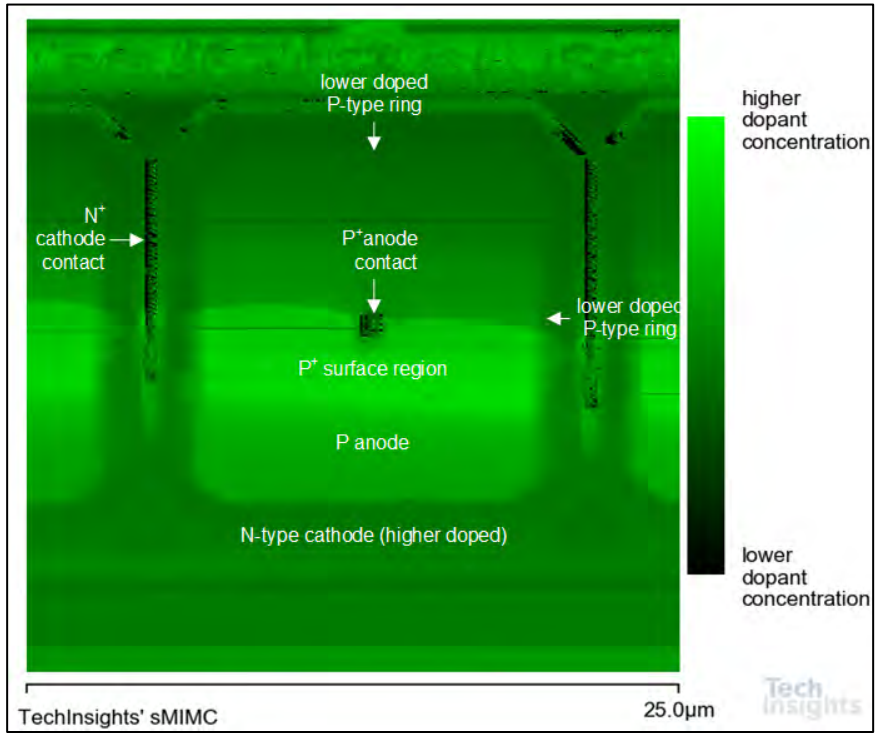
SPAD Planar Analysis

- SCM and SMIM-C images of the SPAD slight below the surface showing the anode and the cathode regions.
- The center region is the anode, and the center of the anode is the higher doped contact. Near the surface the anode is surrounded by a lower doped type guard ring. These images also show that the anode region closer to the surface is P^+ doped, and below it the anode is lower doped.
- The cathode contact region is N^+ doped.



array_032522101657_PRODUCT_FRW_25.0u_512p_390722.png

SPAD Slightly Below the Surface – Planar SCM

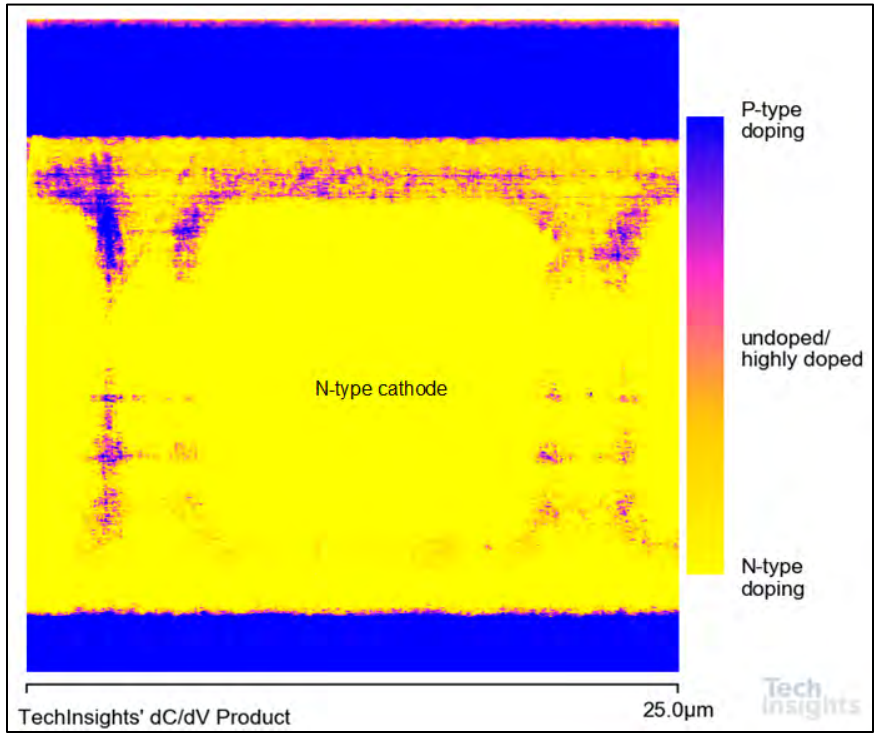


array_032522101657_SMIMC_FRW_25.0u_512p_390722.png

SPAD Slightly Below the Surface – Planar SMIM-C

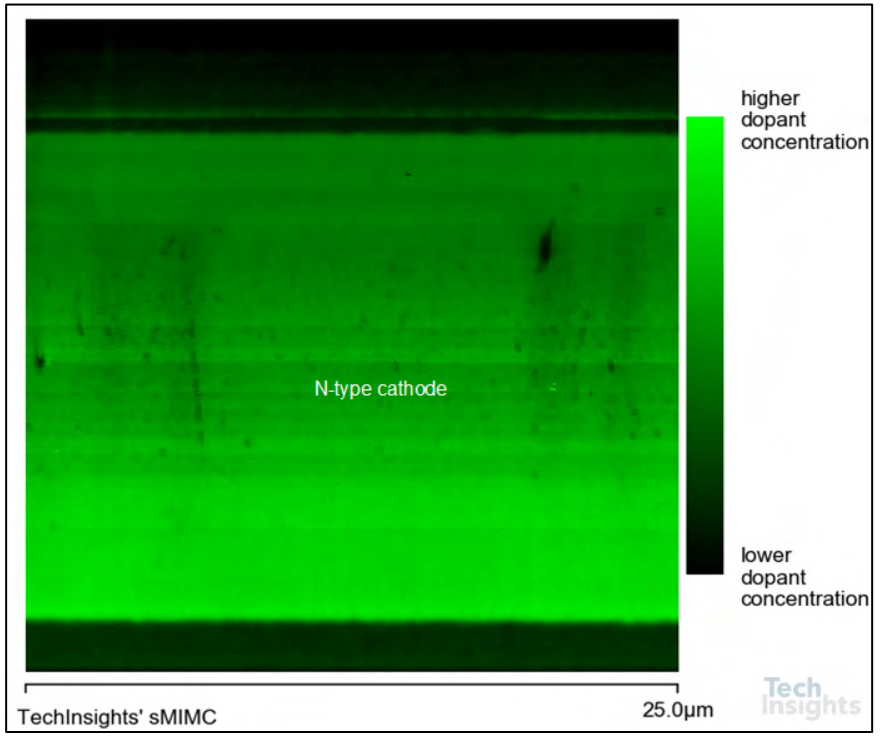
SPAD Planar Analysis

- SCM and SMIM-C images of the SPAD below the anode region.
- At this depth only the N-type cathode is shown.



array_cathode_032822154754_PRODUCT_FRW_25.0u_512p_390722.png

SPAD Below the Anode – Planar SCM



array_cathode_032822154754_SMIMC_FRW_25.0u_512p_390722.png

SPAD Below the Anode – Planar SMIM-C

SPAD Readout Circuitry Plan-View Analysis

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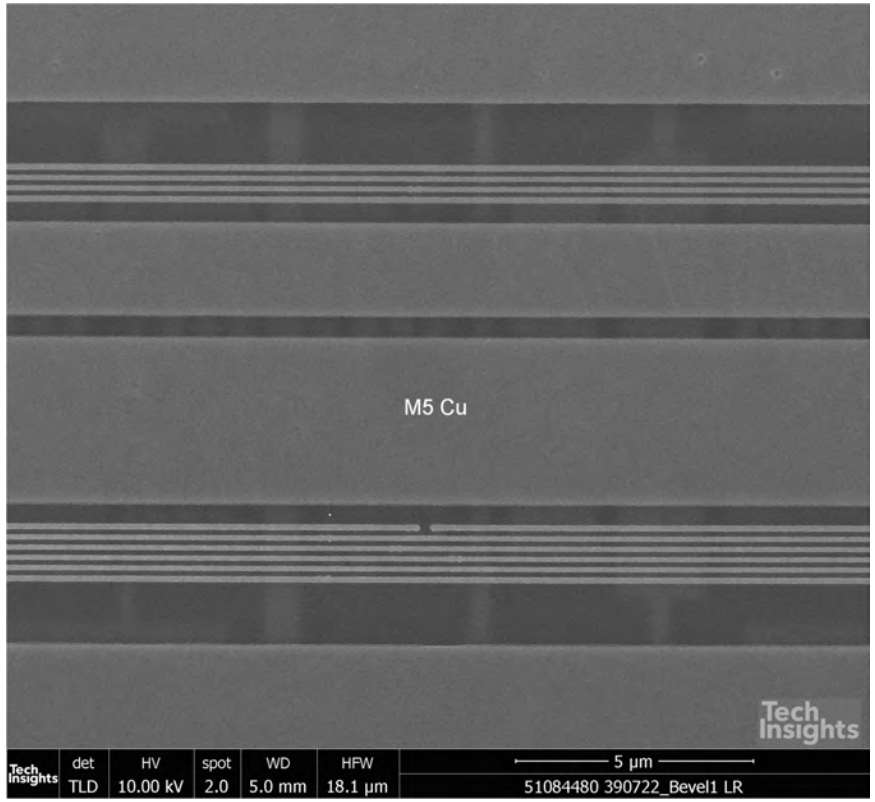
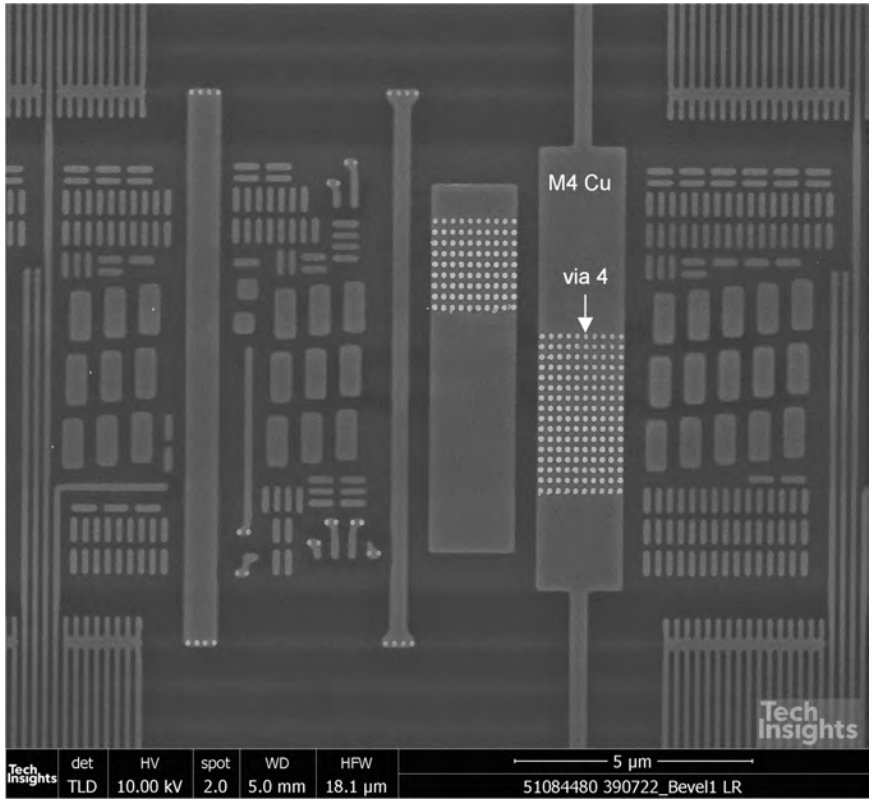
SPAD Readout Circuitry Planar Analysis

- The SPAD readout circuitry at metal 5, metal 4, and via 4.



319_Bevel1_Array_M5_390722.png

SPAD Readout Circuitry at Metal 5 – SEM Plan-View

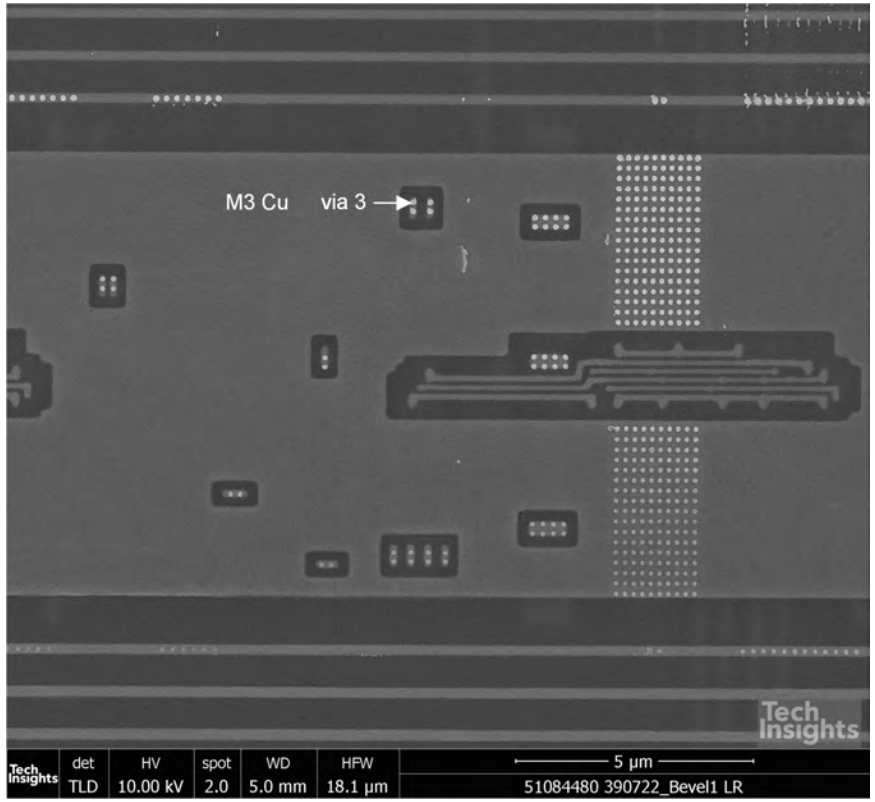


316_Bevel1_Array_M4_390722.png

SPAD Readout Circuitry at Metal 4 and Via 4 – SEM Plan-View

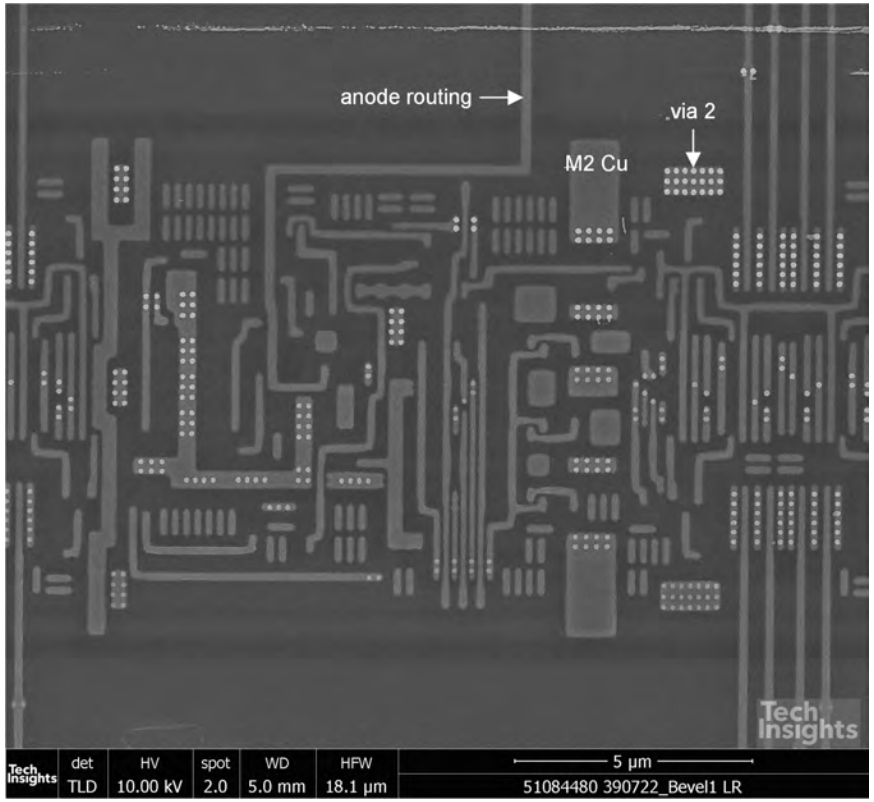
SPAD Readout Circuitry Planar Analysis

- The SPAD readout circuitry at metal 3 and via 3, and metal 2 and via 2.
- The right image shows the routing of the anode signal.



313_Bevel1_Array_M3_390722.png

SPAD Readout Circuitry at Metal 3 and Via 3 – SEM Plan-View

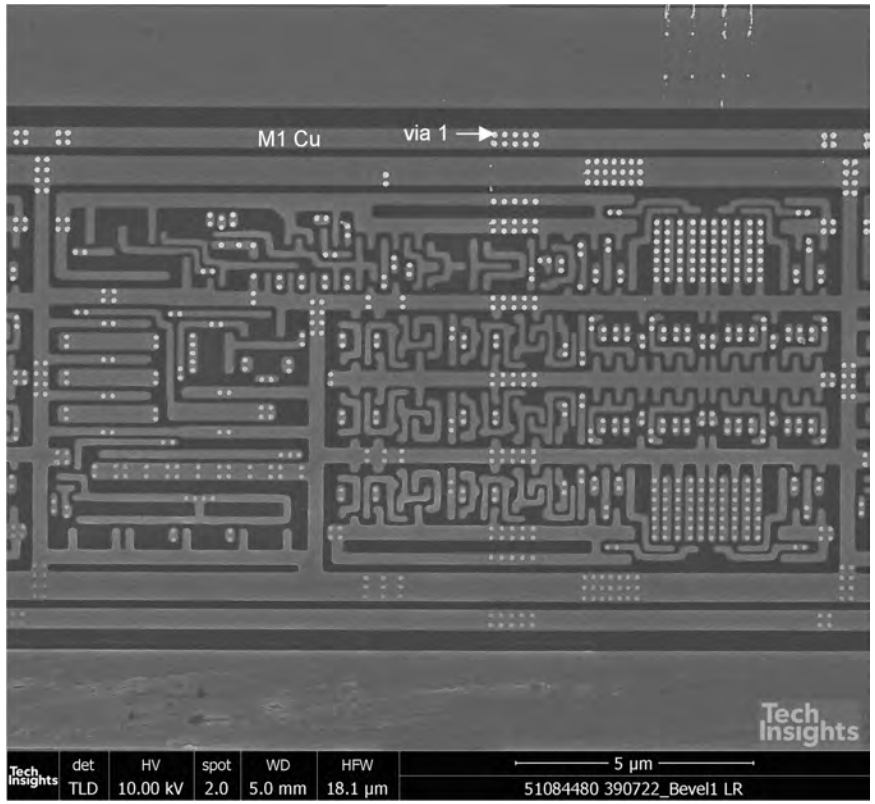


311_Bevel1_Array_M2_390722.png

SPAD Readout Circuitry at Metal 2 and Via 2 – SEM Plan-View

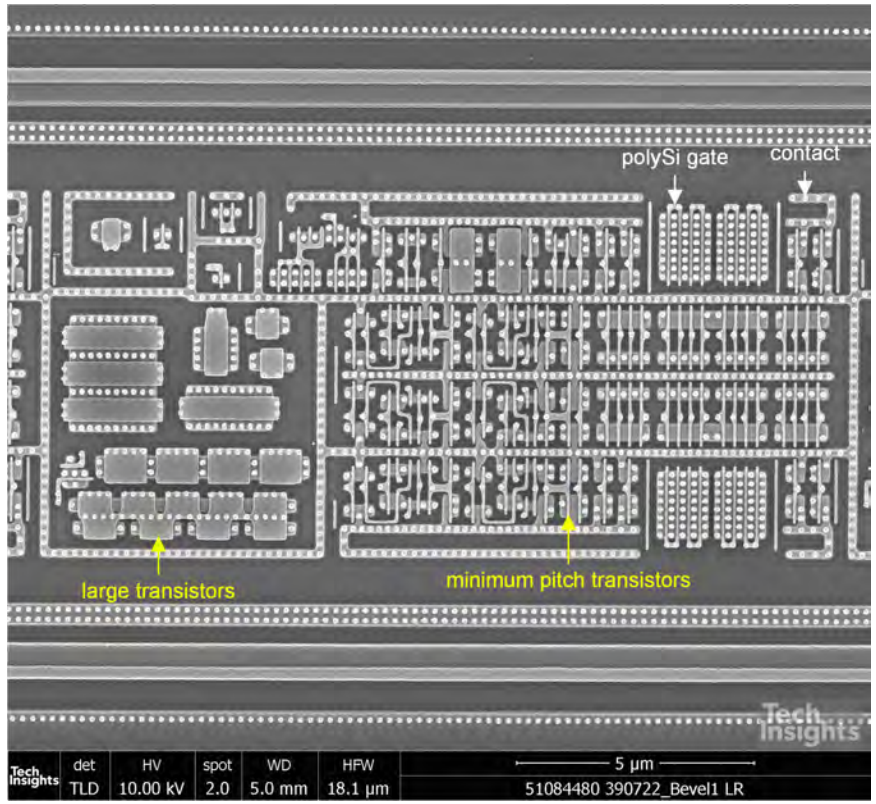
SPAD Readout Circuitry Planar Analysis

- The SPAD readout circuitry at metal 1 and via 1, contact, and polysilicon.



308_Bevel1_Array_M1_390722.png

SPAD Readout Circuitry at Metal 1 and Via 1 – SEM Plan-View

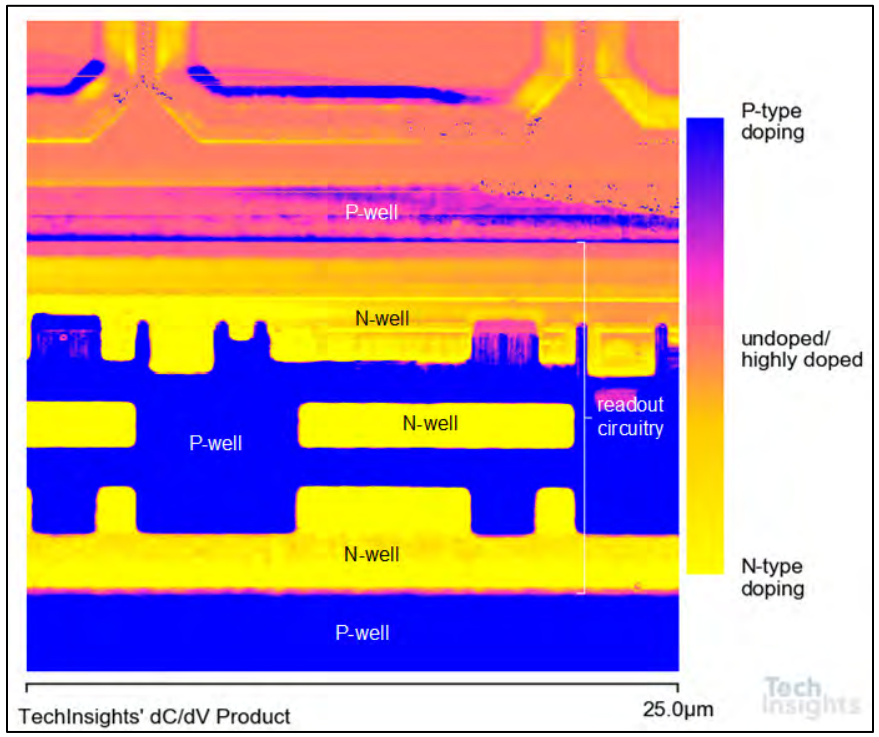


302_Bevel1_Array_Poly_390722.png

SPAD Readout Circuitry at Contact and Polysilicon – SEM Plan-View

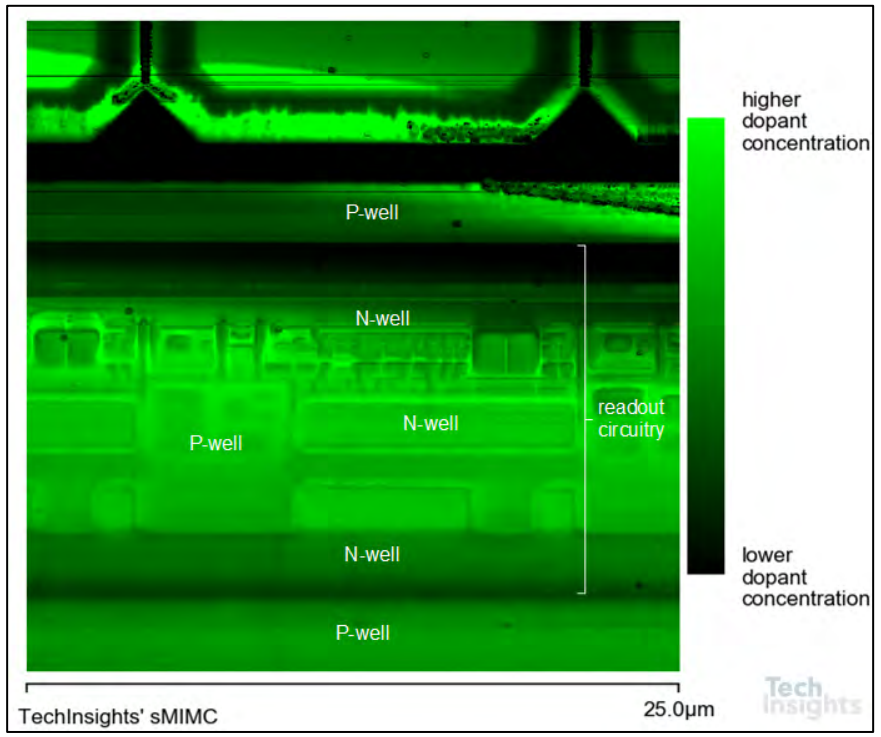
SPAD Readout Circuitry Planar Analysis

- SCM and SMIM-C images of the SPAD readout circuitry showing the N-wells and P-wells.
- There is a P-well separating the SPAD and the readout circuit.



readout_wells_032422141852_PRODUCT_FRW_25.0u_512p_390722.png

SPAD Readout Circuitry N-Well and P-Well – Planar SCM



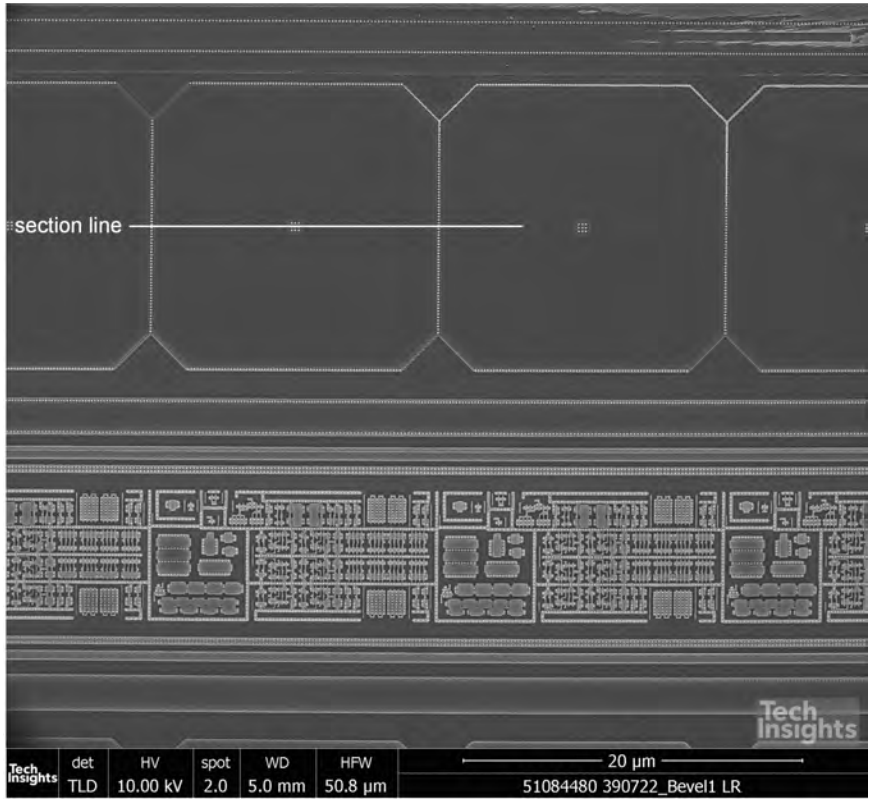
readout_wells_032422141852_SMIMC_FRW_25.0u_512p_390722.png

SPAD Readout Circuitry N-Well and P-Well – Planar SMIM-C

SPAD Cross Section Analysis X-Direction

SPAD Cross Section Analysis

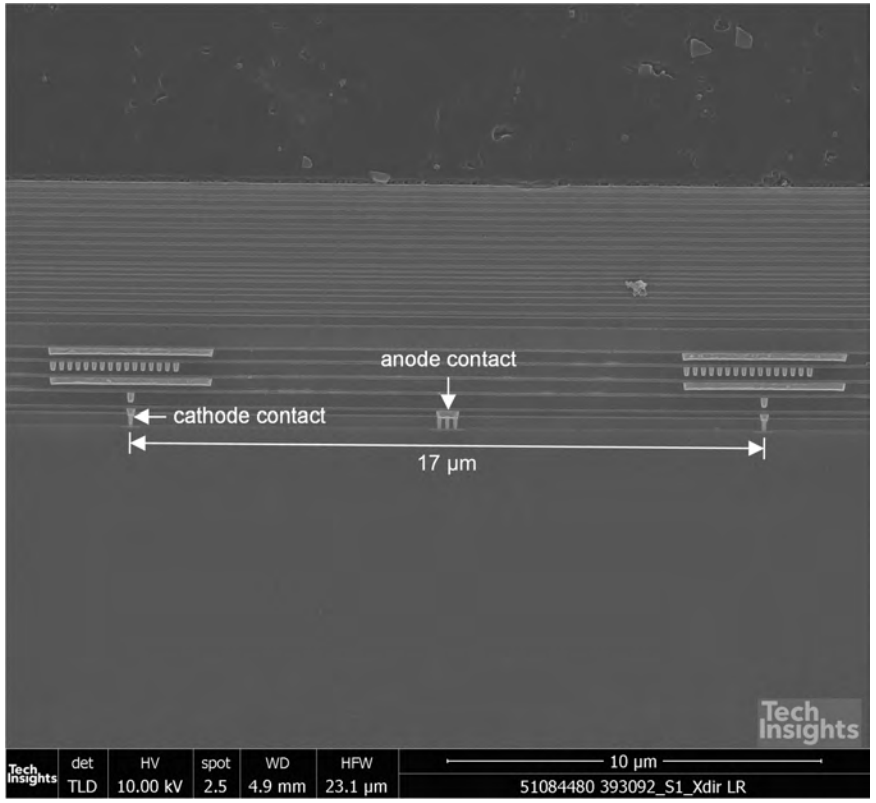
- SEM bevel image at polysilicon and contact showing the main SPAD features, and X-direction cross section plane used to analyze the SPAD structure.



236_Bevel1_Array_390722_X.png

SPAD Cross Section Analysis X-Direction

- SEM cross section image of the SPAD array in the X-direction through the center of the SPAD anode contact.

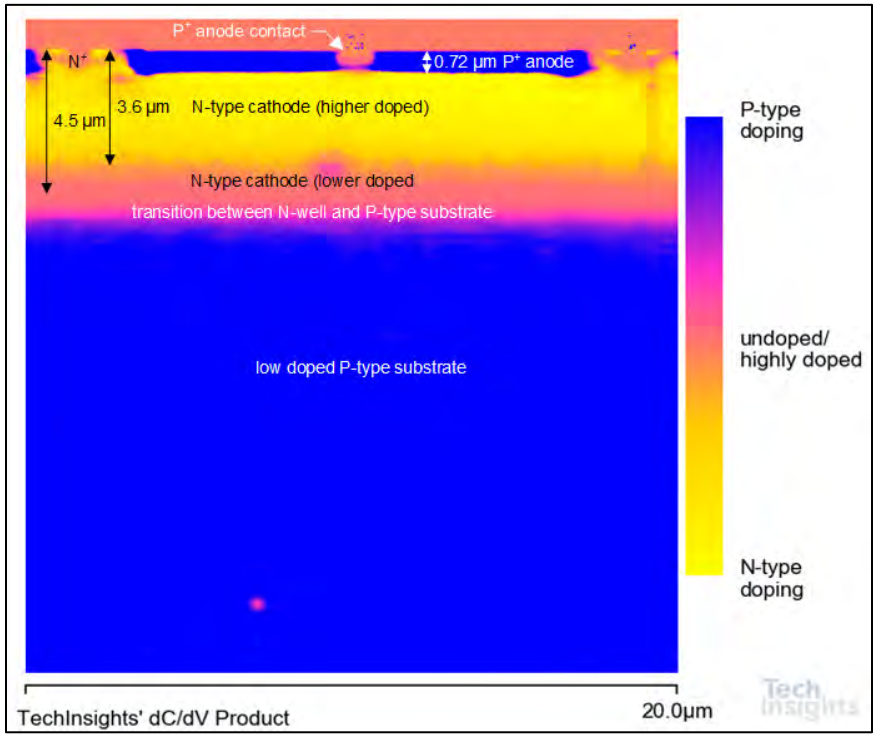


903_Active_Array_Centre_of_SPAD_Pixel_SliceA_393092_1.png

SPAD General Structure Overview – SEM

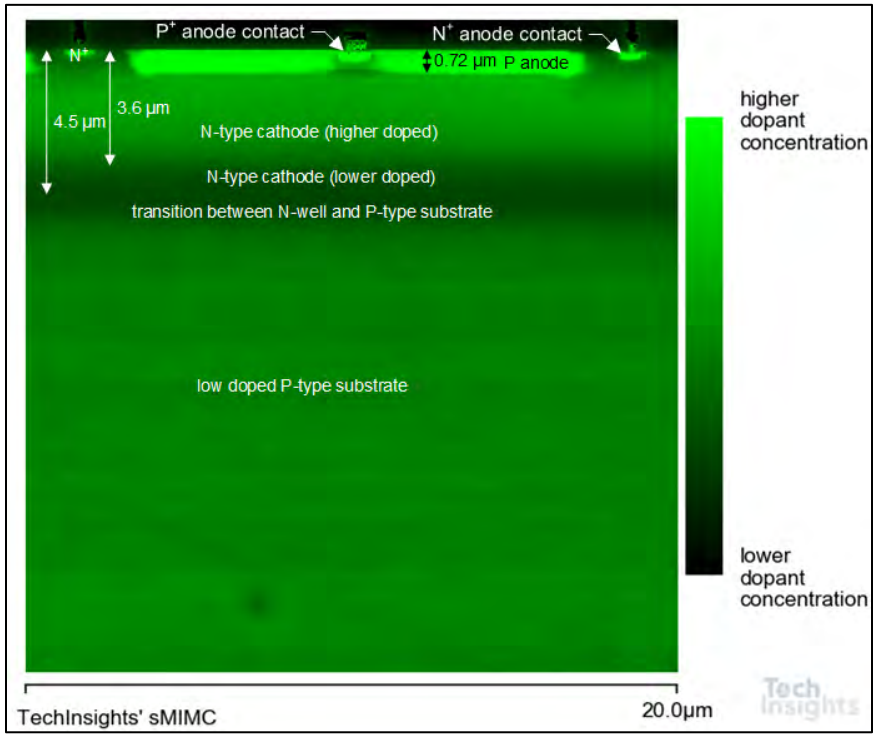
SPAD Cross Section Analysis X-Direction

- SCM and SMIM-C cross section images through the center of the SPAD anode contact.
- The anode is 0.72 µm deep high doped P-type.
- The cathode is about 4.5 µm deep and has an about 3.6 µm deep higher doped upper region and an ~0.90 µm deep lesser doped lower region.



Midpixel_030822164545_PRODUCT_FRW_20.0u_512p_393092.png

SPAD Overview Through the Center of Anode Contact – SCM

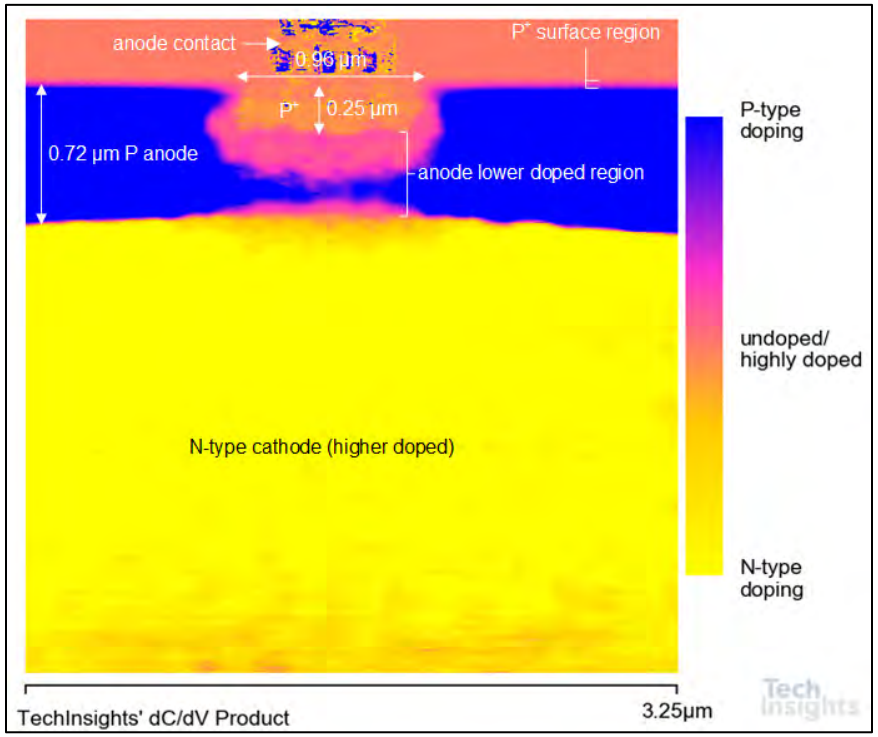


Midpixel_030822164545_SMIMC_FRW_20.0u_512p_393092.png

SPAD Overview Through the Center of Anode Contact – SMIM-C

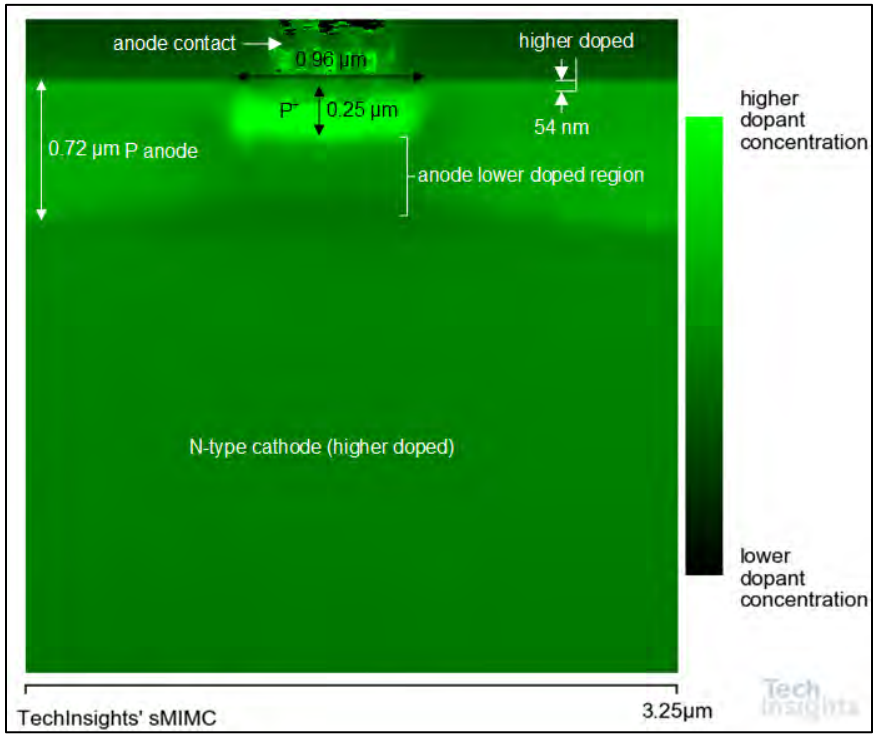
SPAD Cross Section Analysis X-Direction

- SCM and SMIM-C cross section close-up images through the center of the SPAD anode contact.
- The anode contact is a 0.25 µm deep P^+ region, with a lower doped P-type region between the P^+ region and the N-type cathode.
- An ~54 nm deep surface region of the anode is higher doped than the anode body.



Midpixel_030822191807_PRODUCT_FRW_3.25u_512p_393092.png

Anode Contact Detail – SCM

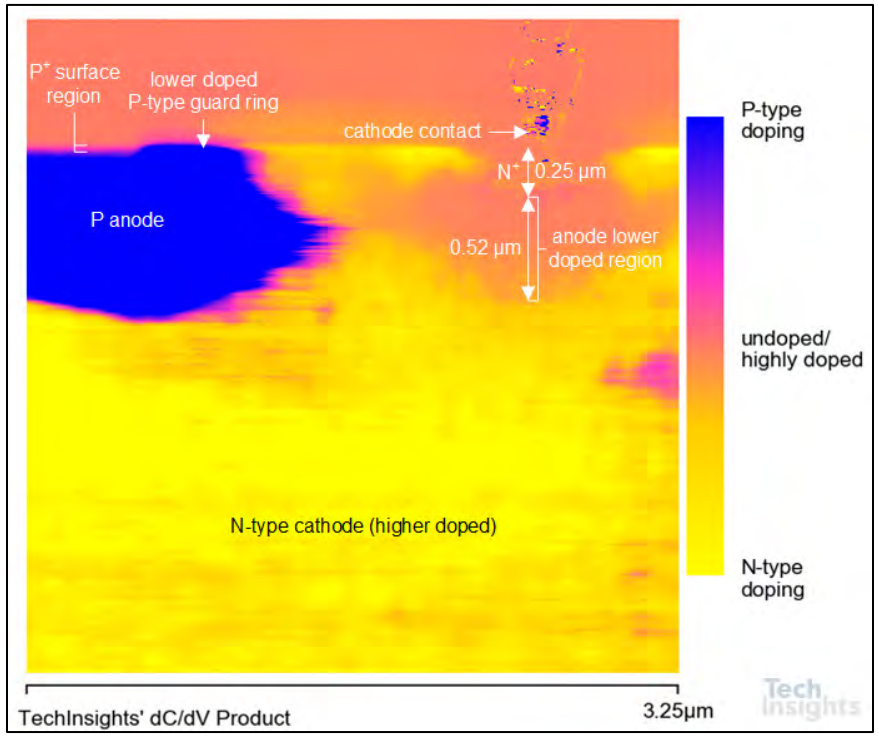


Midpixel_030822191807_SMIMC_FRW_3.25u_512p_393092.png

Anode Contact Detail – SMIM-C

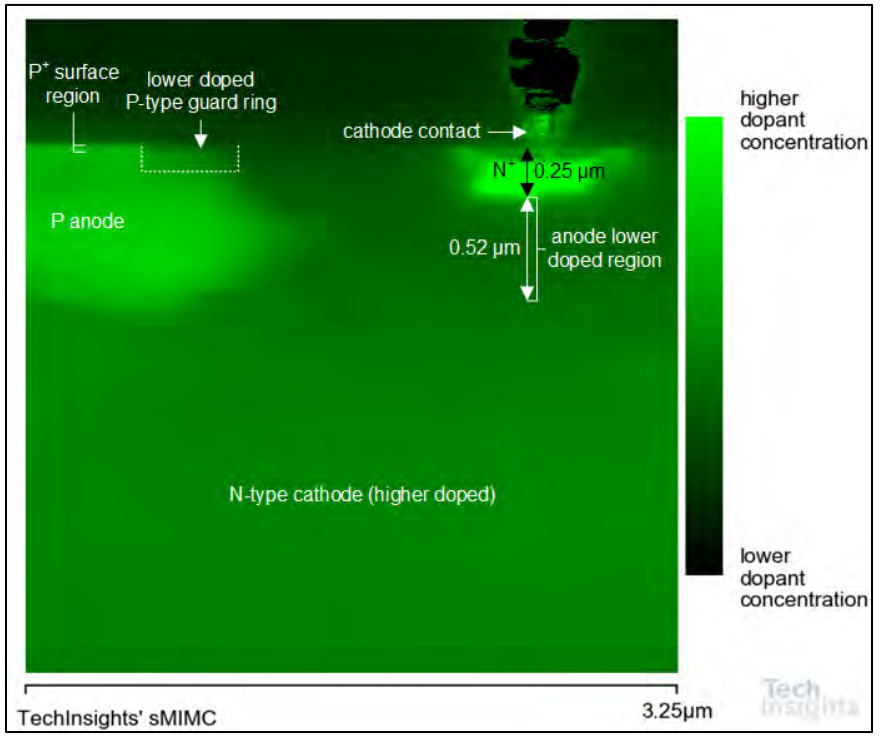
SPAD Cross Section Analysis X-Direction

- SCM and SMIM-C cross section close-up images through the center of the SPAD cathode contact.
- The cathode contact is 0.25 µm deep N^+ region, with a lower doped N-type region below and on the sides.
- At the top edge of the anode there is a lower doped P-type guard ring.



Midpixel_030822185110_PRODUCT_FRW_3.25u_512p_393092.png

Cathode Contact Detail – SCM



Midpixel_030822185110_SMIMC_FRW_3.25u_512p_393092.png

Cathode Contact Detail – SMIM-C

SPAD Cross Section Analysis Y-Direction

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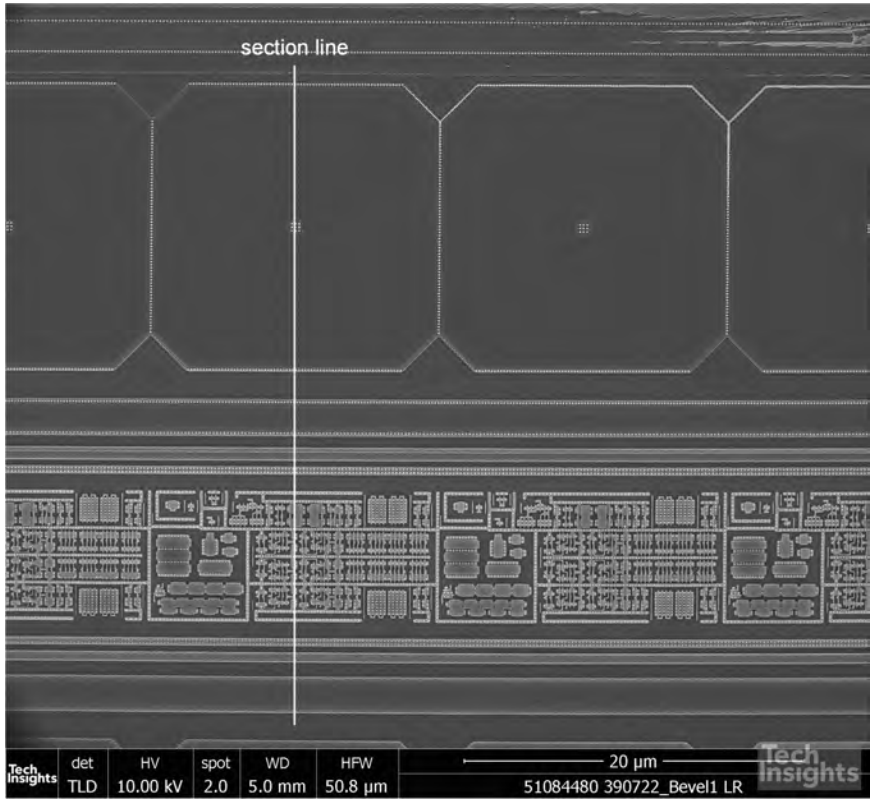
SPAD Cross Section Analysis

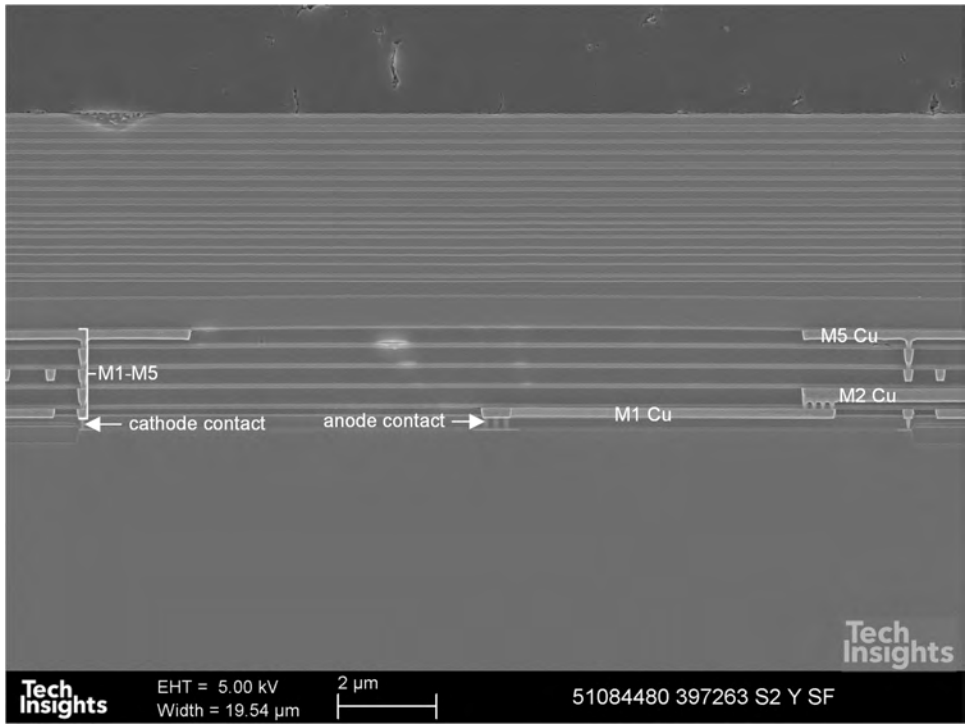
- SEM bevel image at the polysilicon and contact showing the main SPAD features, and Y-direction cross section plane used to analyze the SPAD structure.



236_Bevel1_Array_390722_Y.png

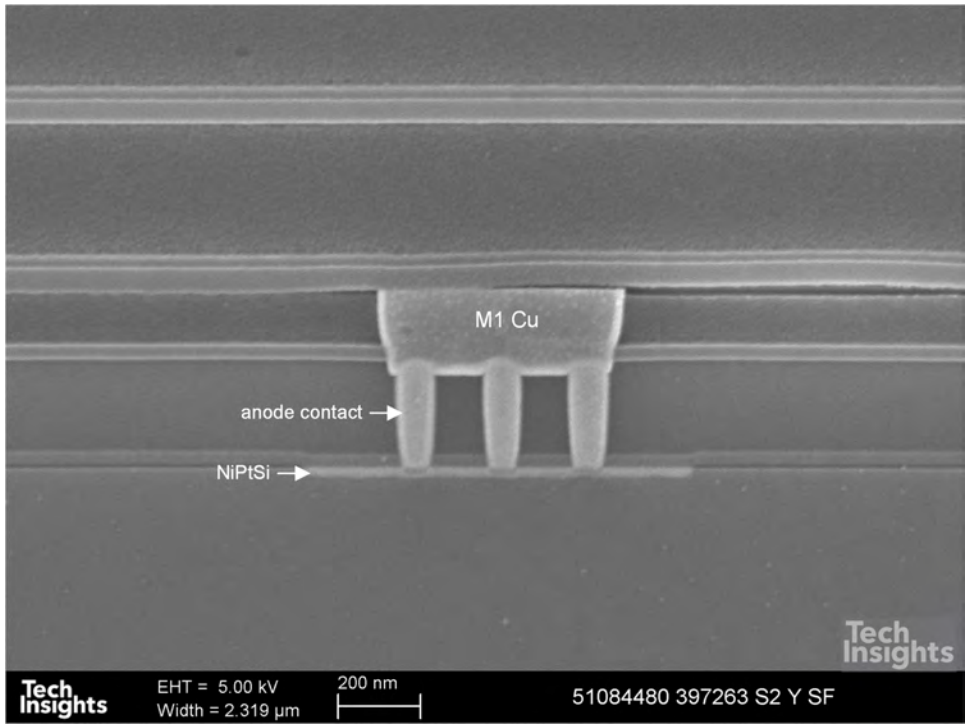
SPAD Cross Section Analysis Y-Direction

- SEM cross section overview and detail images of the SPAD array in the Y-direction through the center of the anode contact.
- The anode contact uses a NiPt silicide.



001_array_SPAD_locD_midpixel_397263.png

SPAD General Structure Overview – SEM

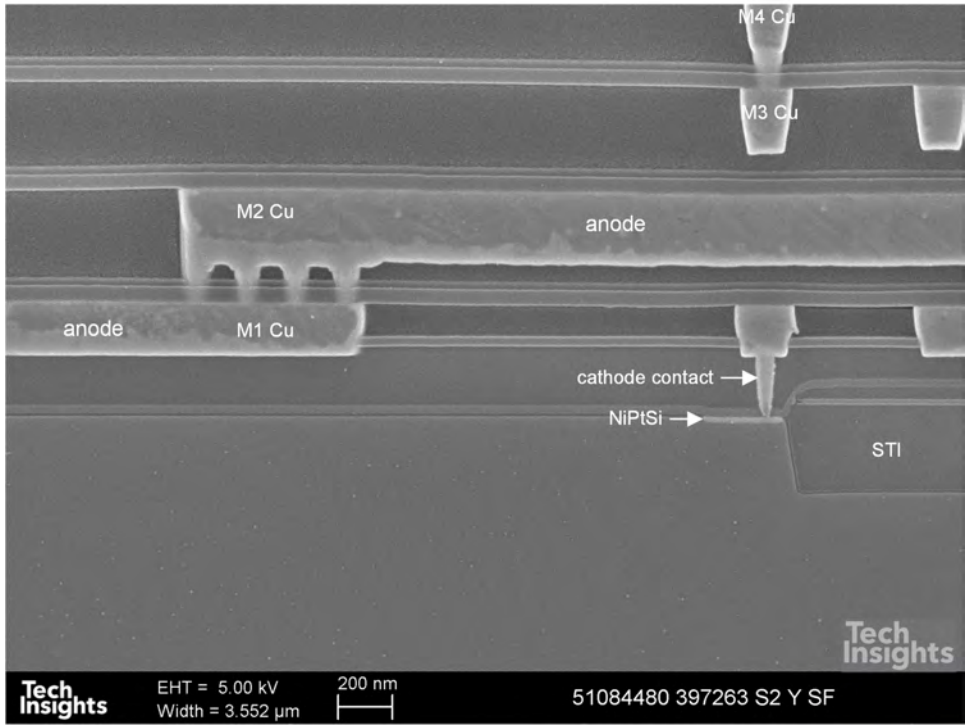


005_array_SPAD_locD_midpixel_397263.png

SPAD Anode Contact Detail – SEM

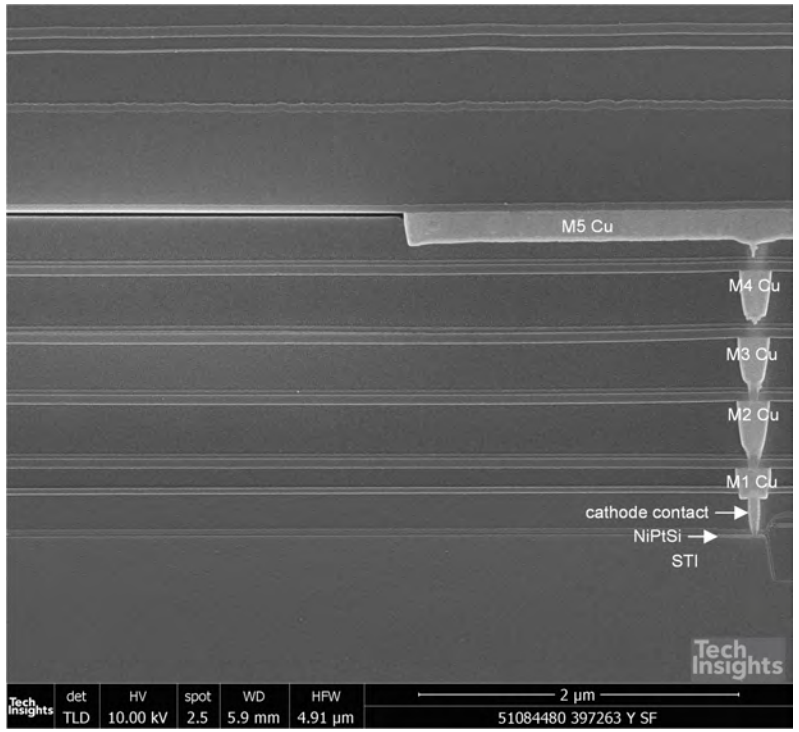
SPAD Cross Section Analysis Y-Direction

- SEM cross section overview and detail images of the SPAD array in the Y-direction through the center of the anode contact.
- The left image shows the detail of the anode signal routing through metal 1 and metal 2.
- The cathode contact is also NiPt silicided.



003_array_SPAD_locD_midpixel_397263.png

SPAD Anode Routing Detail – SEM

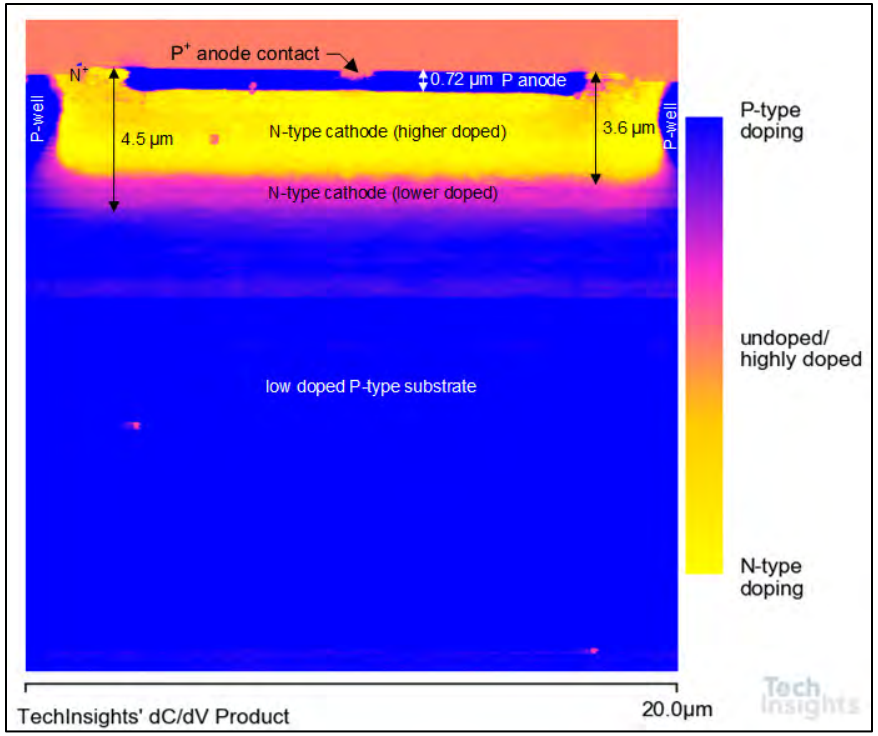


025_array_SPAD_ILDS_397263.png

SPAD Cathode Contact Detail – SEM

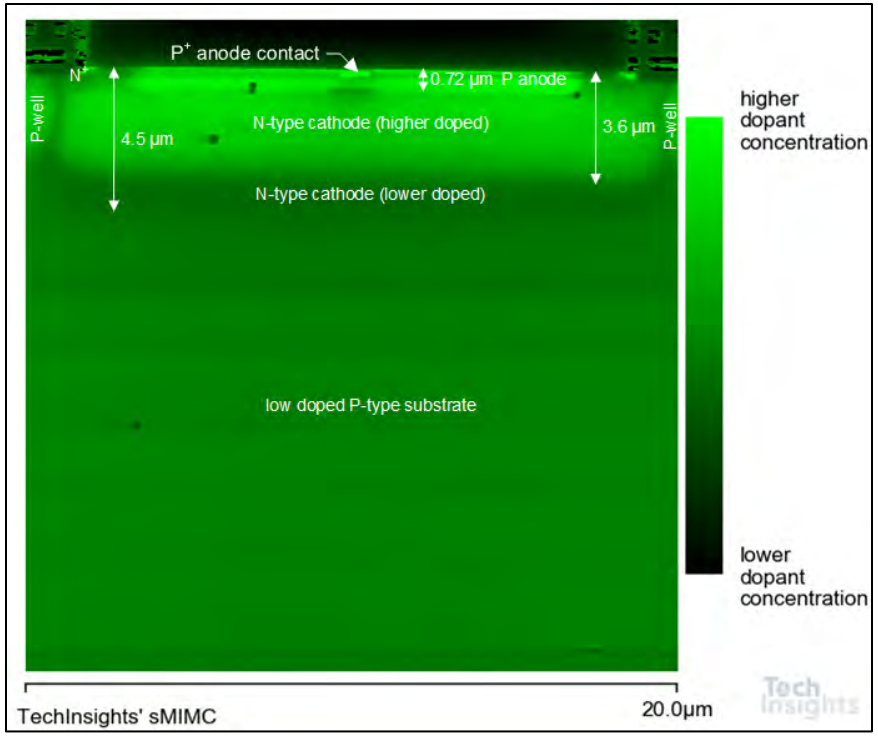
SPAD Cross Section Analysis Y-Direction

- SCM and SMIM-C cross section images in the Y-direction through the center of the SPAD anode contact.
- The anode is 0.72 µm deep high doped P-type.
- The cathode is about 4.5 µm deep and has an ~3.6 µm deep higher doped upper region and an ~0.90 µm deep lesser doped lower region.
- In this direction, on both sides between the SPAD and the readout circuit, there is a P-well.



locD_midpixel_031122165356_PRODUCT_FRW_20.0u_512p_397263.png

SPAD Overview Through the Center of Anode Contact – SCM

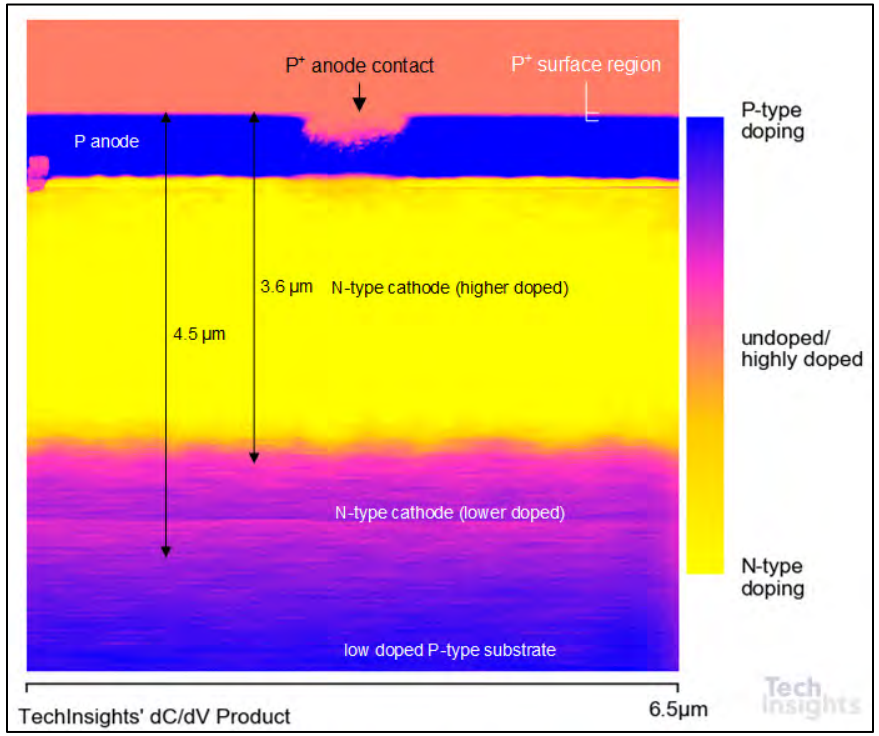


locD_midpixel_031122165356_SMIMC_FRW_20.0u_512p_397263.png

SPAD Overview Through the Center of Anode Contact – SMIM-C

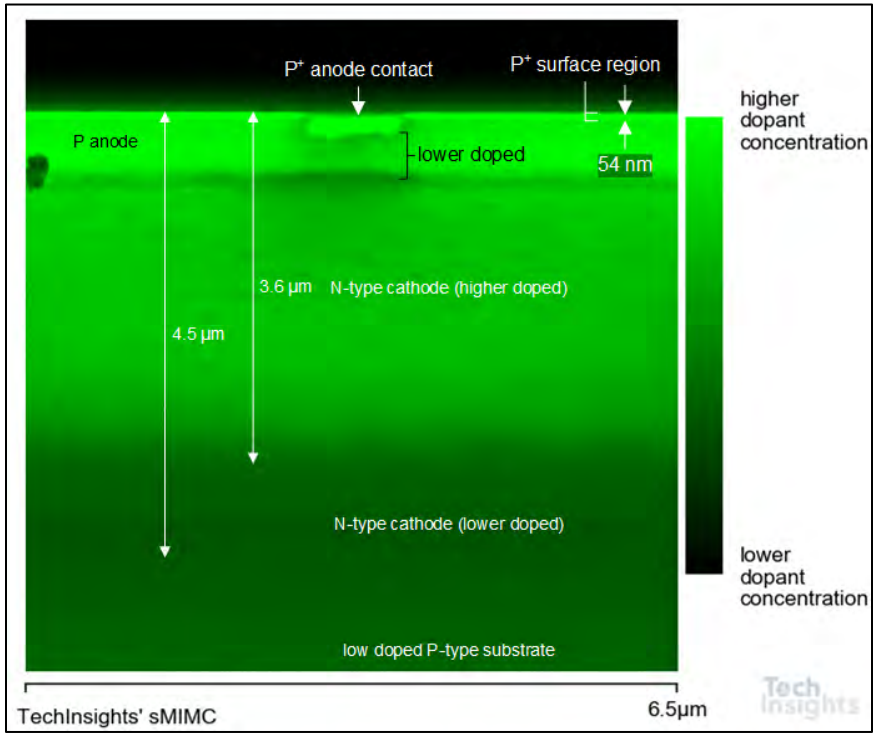
SPAD Cross Section Analysis Y-Direction

- SCM and SMIM-C cross section close-up images through the center of the SPAD anode contact.
- The anode contact is P^+ doped, with a lower doped P-type region between the P^+ region and the N-type cathode.
- An approximate 54 nm deep surface region of the anode is higher doped than the remaining anode body.



locD_midpixel_031122175930_PRODUCT_FRW_6.5u_512p_397263.png

Anode Contact Detail – SCM

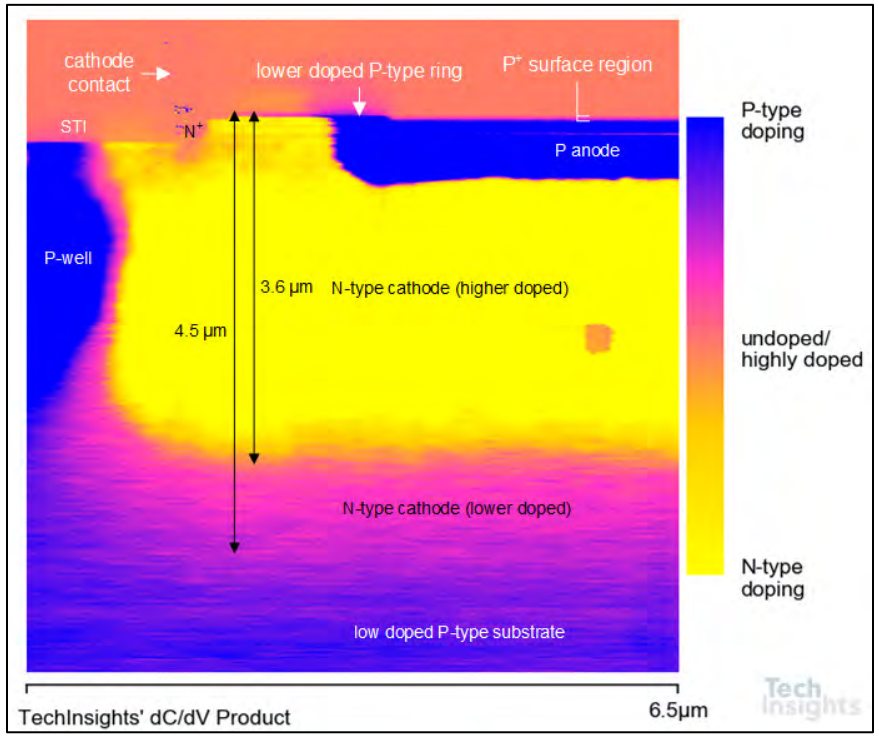


locD_midpixel_031122175930_SMIMC_FRW_6.5u_512p_397263.png

Anode Contact Detail – SMIM-C

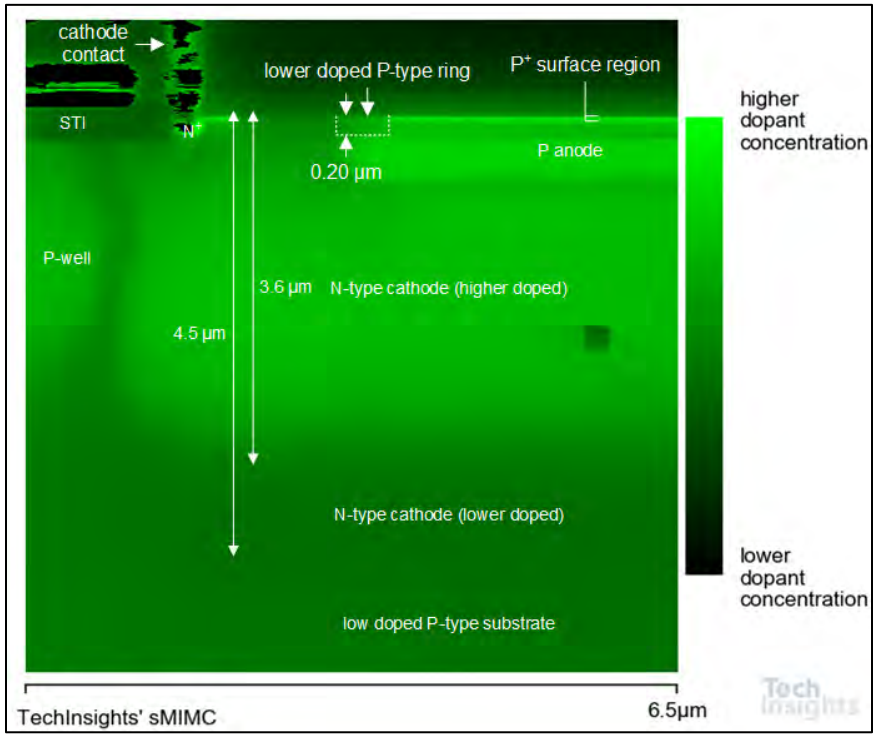
SPAD Cross Section Analysis Y-Direction

- SCM and SMIM-C cross section close-up images through the center of the SPAD anode contact.
- The cathode contact is N^+ region, with a lower doped N-type region surrounding it.
- At the top edge of the anode there is a lower doped P-type guard ring.
- In this direction, on both sides between the SPAD and the readout circuit there is a P-well.



locD_midpixel_031122173351_PRODUCT_FRW_6.5u_512p_397263.png

Cathode Contact Detail – SCM



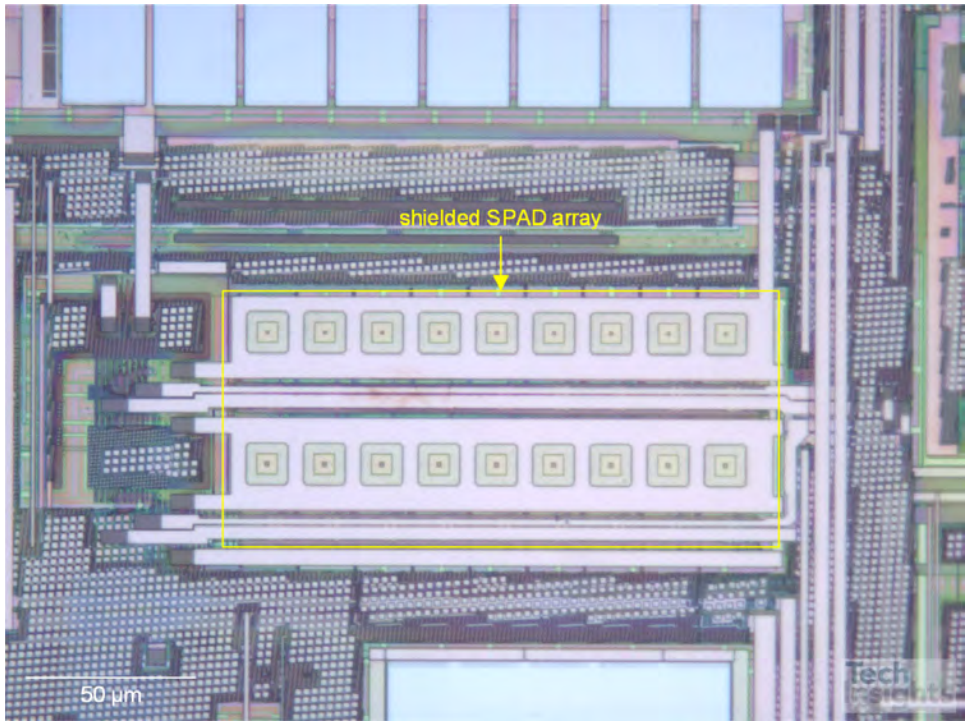
locD_midpixel_031122173351_SMIMC_FRW_6.5u_512p_397263.png

Cathode Contact Detail – SMIM-C

Shielded SPAD Array

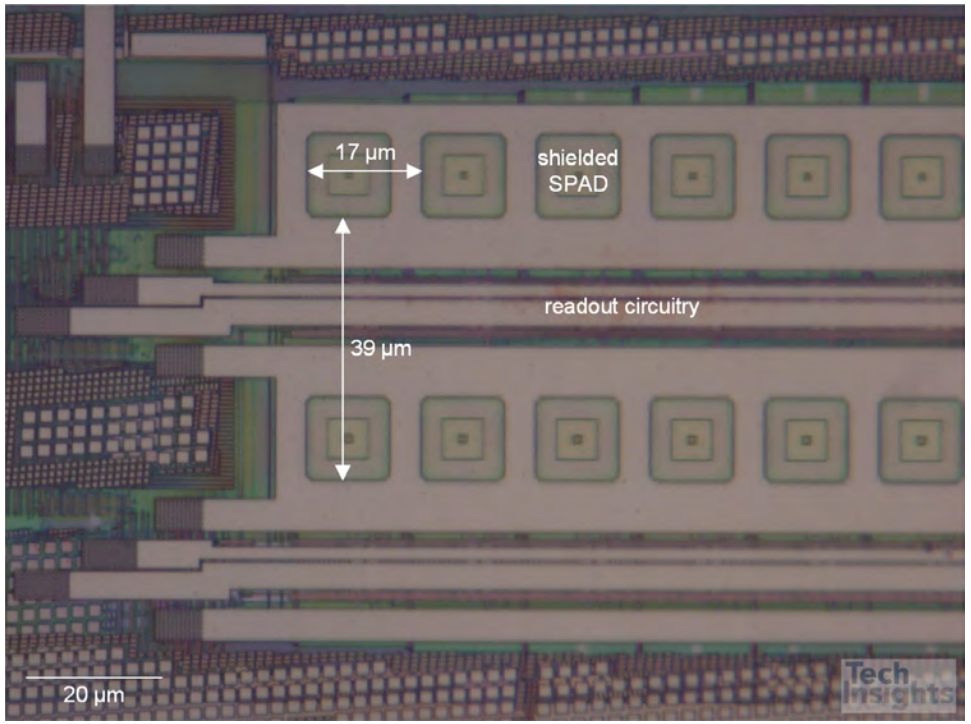
Shielded SPAD Array

- The shieled SPAD array is organized in two rows by nine columns (total 18 SPADs).
- The SPAD pitch is the same as the active SPAD 17 µm × 39 µm.



09 50x1r_391407.png

Shielded SPAD Array Overview – Optical

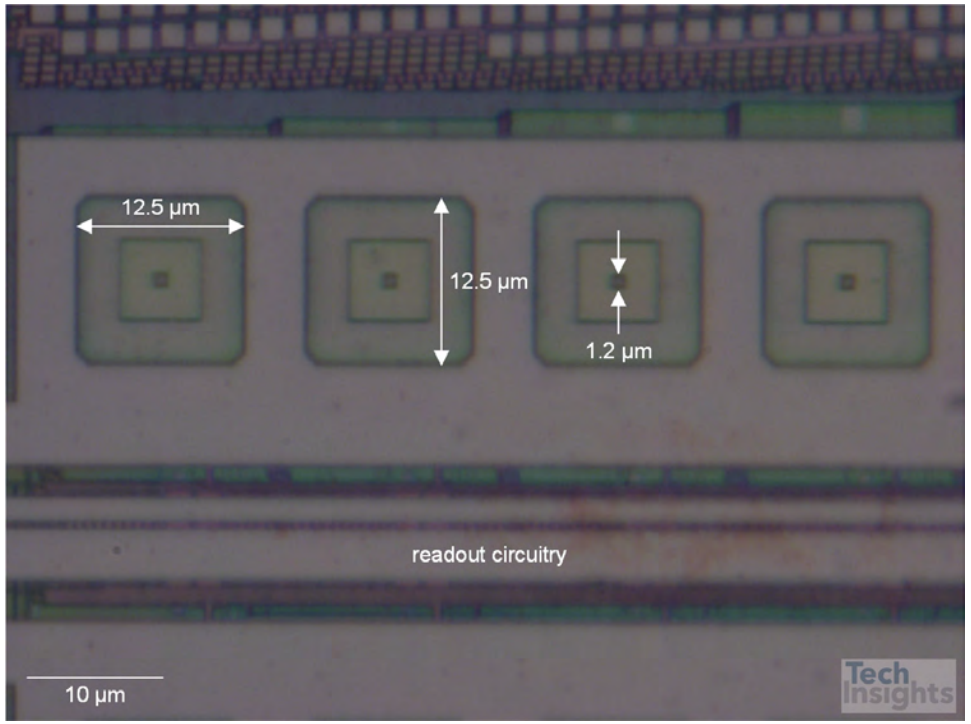


13 100x1r_391407.png

Shielded SPAD Array Close-Up – Optical

Shielded SPAD Array

- The shielded SPAD top metal has an opening of 12.5 µm × 12.5 µm.
- It seems that lower metal layers have progressively smaller openings, with the smallest having an opening of about 1.2 µm square.



14 100x2r_391407.png

Shielded SPAD Array Detail – Optical

References

[1] “TMF8828 configurable 8x8 multi-zone Time-of-Flight Sensor,” https://ams.com/en/tmf8828 accessed on March 30, 2022

[2] “Honor Magic 3 Series,” https://www.hihonor.com/global/phones/honor-magic3-pro-series/ accessed on March 30, 2022

[3] “ams OSRAM TMF8828 d-ToF Rear Facing Sensor from the Honor Magic3 Pro Package Analysis Summary,” *TechInsights*, PKG-2110-801, December 23, 2021

[4] “ams further expands Singapore manufacturing capacity to address global demand for optical sensor solutions,” https://ams.com/en/-/ams-further-expands-singapore-manufacturing-capacity-to-address-global-demand-for-optical-sensor-solutions, accessed on April 6, 2022

Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm (± 1.4%) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within ± 2% of this standard, over the full magnification ranges used.

TechInsights' optical microscopes are calibrated using a stage micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of 0.3 µm (0.3%) for the stage micrometer's 100 µm pitch lines.

Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately ± 5% or better for features larger than about 20% of the image width.

TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers.

The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis is usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration.

Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (sMIM) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request.

Statement of Scope Variation

Due to the nature of reverse engineering and the diversity of analyzed devices, there is a possibility of content variation in TechInsights technical reports.

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